Time-Domain CMOS Temperature Sensors With Dual Delay-Locked Loops for Microprocessor Thermal Monitoring

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***Abstract*—We report on CMOS temperature sensors that work by measuring temperature-dependent delays in CMOS inverters. Two new features distinguish this work from the prior delay-based temperature sensors. First, our sensor operates with simple, low-cost one-point calibration. Second, it uses delay-locked loops (DLLs) to convert inverter delays to digital temperature outputs: the use of DLLs enables low energy (0.24 μJ/sample) and high bandwidth (5 kilo-samples/s), facilitating fast thermal monitoring. After calibration, measurement errors for 15 chips fabricated in digital CMOS 0.13 μm fall within $-4.0 \sim 4.0\,^{\circ}$C in a temperature range of $0 \sim 100\,^{\circ}$C, where the temperature chamber used has a control uncertainty of $\pm 1.1\,^{\circ}$C. Microprocessor thermal profiling can be a potential application.**

***Index Terms*—CMOS, delay locked loops (DLLs), microprocessors, temperature sensors, time-to-digital converters (TDCs).**

I. Introduction

TODAY's microprocessors increasingly exhibit temperature variations across their dice [1]–[7]. To counter the resulting performance deterioration, the thermal profile of a microprocessor can be monitored using integrated temperature sensors distributed across the microprocessor, and local power dissipations can be adaptively adjusted according to the thermal profile [1]–[6].

A well-established and successful paradigm for integrated temperature sensors exploits the temperature dependence of base-emitter voltages of bipolar transistors [8]–[17]. For example, in Fig. 1(a) the difference between base-emitter voltages (ΔV_{BE}) of two bipolar transistors biased at two different currents (I_1, I_2) is proportional to temperature. This voltage difference is compared to a temperature-independent bandgap voltage reference (V_{REF}) by an analog-to-digital converter (ADC), and mapped to a digital temperature output.

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More recently there appeared a new type of integrated temperature sensors that exploit the temperature dependence of time delays of CMOS inverters [18]–[21]. A time-to-digital converter (TDC) compares the temperature-dependent delay of an inverter chain to a temperature-independent delay reference (e.g., crystal oscillator) to produce a digital temperature output [see Fig. 1(b)]. The inverter delay, delay reference, and TDC are analogous to the base-emitter voltage, bandgap reference, and ADC of the conventional sensor.

Needing improvements in various aspects, whether the delay-based sensors can be a viable practical option remains to be seen, subject to further study. They can be potentially well suited for microprocessor thermal profiling, as they are more digital and do not need parasitic bipolar transistors. Here we report a CMOS delay-based temperature sensor intended for the microprocessor thermal profiling. It builds up from the original delay-based CMOS temperature sensor work of [18]–[21], with the following two new key features.

1) Since the inverter delay varies not only with temperature but also with process variation, the temperature dependence of the delay differs from sensor to sensor. Therefore, each sensor needs calibration according to its process variation. The prior delay-based sensors [18]–[21] measure delays at two known temperature points to calibrate out process variations. By contrast, our sensor operates with simple one-point calibration, which is the first key feature of our work. The one-point calibration may not produce as accurate temperature measurements as the two-point calibration, but is simpler, thus, reduces high-volume production cost. This choice of trade-off is meaningful in the microprocessor application, where high precision is not required but lower calibration cost is desirable. The latter is because temperature sensors play auxiliary, albeit important, roles without taking part in main computing activity. The one-point calibration is enabled by our observation that the inverter delay can be separated into a function of temperature only and a function of process only.
2) The prior delay-based temperature sensors [see Fig. 1(b)] [18]–[21] measure inverter delays using a counter-based cyclic TDC and a single temperature-independent delay reference. The second key feature of our work is the architectural modification of Fig. 1(b) by using two delay-locked loops (DLLs). One DLL synthesizes multiple temperature-independent delay references; the other DLL serves as a TDC, and compares temperature-dependent inverter delays to the multiple delay references

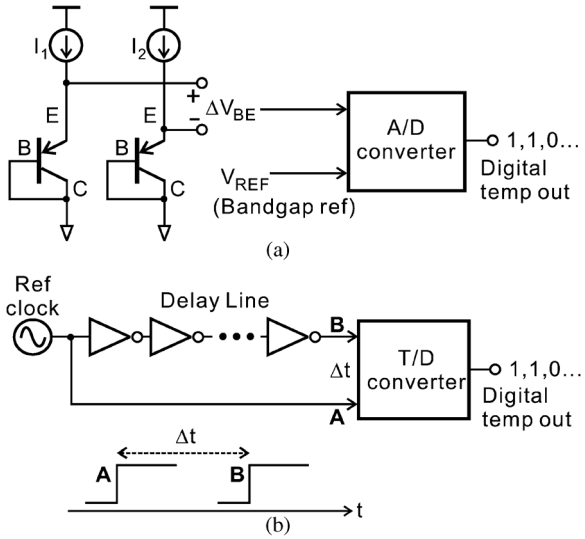

Fig. 1. (a) Conventional temperature sensor using bipolar transistors. (b) Inverter-delay-based temperature sensor.

synthesized by the first DLL. Crystal oscillators required by DLLs are readily available in microprocessor environment. The use of multiple delay references via DLLs leads to a high bandwidth (5 kilo-samples/s) at 7-bit resolution, which can facilitate tracking of fast thermal transients.

This work was partially reported in [25]. This paper is a significant expansion with new substantial experiments with an increased number of sensor chips (5 chips versus 15 chips) and new analyses. Sections II and III describe in details the two new features of our sensor, thus, its operating principles. Section IV presents design implementation. Section V reports measurements of fabricated CMOS sensors to validate the principle, and compares the performance of our sensor to that of the prior delay-based temperature sensors.

Delay-based CMOS temperature sensors are prone to high sensitivity to static supply shift [18]–[21]. Our design here also does not overcome this issue. We explicitly measure and quantify the sensitivity of our sensor to static supply shift to motivate further studies. This is presented in Section VI.

II. Operating Principle (1)—One-Point Calibration

A. Inverter Delay and Separation of Variables

Separation of the CMOS inverter delay into a function of only temperature and a function of only process parameters is a key to our one-point calibration. Here we establish this separation of variables. Consider a CMOS inverter with equivalent pMOS and nMOS strengths. The propagation delay, D, through the CMOS inverter may be expressed as [26]

$$D = \frac{L}{W}\frac{C_L}{C_{\rm ox}} \cdot \frac{1}{\mu} \cdot \frac{\ln\{3 - 4V_{\rm th}/V_{\rm dd}\}}{V_{\rm dd}(1 - V_{\rm th}/V_{\rm dd})}. \tag{1}$$

C_L is the load capacitance and $V_{\rm dd}$ is the supply. L and W are the gate length and width, μ is the mobility, $C_{\rm ox}$ is the gate oxide capacitance per unit area, and $V_{\rm th}$ is the threshold voltage, all for the nMOS transistor. We will demonstrate the separation of variables using (1). Although we use short-channel transistors in our design, we chose this expression derived from long-channel transistors for simplicity. As discussed in Section II-C, the essence of our analysis remains valid for short-channel device cases.

In (1), μ and $V_{\rm th}$ are the only temperature-dependent parameters to the first order. For temperatures in excess of 200 K, the temperature dependence of μ may be experimentally fitted to [27], [28]

$$\mu(T) \approx \mu(T_0)\left(\frac{T}{T_0}\right)^{\alpha}. \tag{2}$$

T is temperature; T_0 and $\alpha(<0)$[1] are fitting constants. With increasing T, silicon lattice vibrates more, increasing electron scattering, thus, reducing the mobility, as captured in (2).

$V_{\rm th}$'s temperature dependence may be expressed as [29]:

$$V_{\rm th}(T) \approx V_{\rm th}(T_0) + \beta(T - T_0). \tag{3}$$

With proportional constant β on the order of mV/K, $V_{\rm th}$ does not vary with T as much as μ does. Moreover, in (1), $V_{\rm th}$ always appears in the form of $V_{\rm th}/V_{\rm dd}$ where $V_{\rm th}$ is a fraction of $V_{\rm dd}$. Overall, $V_{\rm th}$ does not affect the temperature dependence of the inverter delay D as much as μ: we estimate that the temperature dependence of D due to $V_{\rm th}$ is a few percent of that due to μ, when T changes from 0 to 100 °C.

Therefore, we may neglect $V_{\rm th}$'s temperature dependence and consider only μ to account for the temperature dependence of D. Equation (1) then can be rewritten as

$$D(T, P) = \left(\frac{T_0}{T}\right)^{\alpha} \cdot G(P) \tag{4}$$

where $G(P)$ is defined as

$$G(P) \equiv \frac{L}{W}\frac{C_L}{C_{\rm ox}} \cdot \frac{1}{\mu(T_0)} \cdot \frac{\ln\{3 - 4V_{\rm th}/V_{\rm dd}\}}{V_{\rm dd}(1 - V_{\rm th}/V_{\rm dd})} \tag{5}$$

and P collectively denotes process variations. Eq. (4) emphasizes the separation of the inverter delay into the temperature-dependent function $(T_0/T)^{\alpha}$ and the temperature-independent function $G(P)$, while the latter is a function of process variations.

Furthermore, the temperature-dependent function $(T_0/T)^{\alpha}$, originating from the mobility, exhibits negligible dependence on process variations. The exponent α, affected by the electron scattering due to impurity sites, varies with doping level [30]: e.g., as the doping level changes by orders of magnitude from $10^{14}/{\rm cm}^3$ to $10^{17}/{\rm cm}^3$, α varies only from -2.2 to -1.5. Thus doping level variations typically moderate within a given technology would alter α only slightly. Consequently $(T_0/T)^{\alpha}$ in (4) negligibly depends on process variations.

Therefore, we can rewrite (4) into

$$D(T, P) = F(T) \cdot G(P) \tag{6}$$

where

$$F(T) \equiv \left(\frac{T_0}{T}\right)^{\alpha}. \tag{7}$$

Equation (6) shows the separation of inverter delay into temperature-only-dependent function $F(T)$ and process-only-dependent function $G(P)$. Separation of variables has been obtained.

[1]alpha's numerical values, typically $-2.2 \sim -1.5$, are discussed shortly.

B. Principle of One-Point Calibration

Since the inverter delay depends on both temperature and process variation, the effect of the process variation should be calibrated out, in order to extract temperature information from a measured delay. The separation of variables in the inverter delay enables calibration with a delay measurement only at one known temperature (one-point calibration). We first set temperature at $T = T_c$ (subscript "c" denotes "calibration") and measure the inverter delay $D(T_c, P)$

$$D(T_c, P) = F(T_c) \cdot G(P). \tag{8}$$

We then measure the delay at an unknown temperature T we seek to find out, yielding $D(T, P)$ of (6). Dividing $D(T, P)$ by $D(T_c, P)$, we obtain a *normalized delay* at T

$$D_{\text{norm}}(T) \equiv \frac{D(T, P)}{D(T_c, P)} = \frac{F(T) \cdot G(P)}{F(T_c) \cdot G(P)} = \left(\frac{T_c}{T}\right)^{\alpha}. \tag{9}$$

Since the process dependency $G(P)$ has been canceled out, the normalized delay is a function of temperature only. Therefore, the normalized delay is reproducible across different process corners, serving as a faithful temperature representation. This is the foundation of our one-point calibration scheme.

Simulations with 0.13 μm CMOS validate our one-point calibration approach. We simulated propagation delays of a delay buffer (two minimum-sized inverters in series, with a fan-out-two load) with varying temperatures and process corners. Fig. 2(a) shows simulated absolute delay versus temperature in various process corners, which corresponds to (6). From these results, we can obtain normalized delay versus temperature in various process corners as shown in Fig. 2(b), which corresponds to (9), where $T_c = 50\,^{\circ}\text{C}$. Although the absolute delay in the slow corner is almost twice that in the fast corner [see Fig. 2(a)], normalized delays remain almost the same across all process corners [see Fig. 2(b)].

Normalized delays in Fig. 2(b) still exhibit non-zero variations across different process corners towards 0 °C and 100 °C. This corresponds to an error of ±2.8 °C [see Fig. 2(c)]. This is because the separation of variables, (6), is a first-order approximation. In reality, V_{th}, and thus, $G(P)$, is a weak function of temperature. Hence, the process dependency is not completely removed in normalized delays, causing the error. This error due to the approximate nature of the separation of variables is the fundamental limit to our sensor accuracy. The one-point calibration comes at the price of somewhat reduced accuracy, which, however, is deemed sufficient for microprocessor thermal profiling [5], [6], [31]–[33]. In addition, the simplicity of the one-point calibration is a desirable aspect in the microprocessor application, as stated in Section I.

C. Remarks

Although Section II-A obtained the separation of variables using long-channel transistors, as it is analytically more tractable, the same may be done in principle, albeit complicated, for short-channel transistors. This is because the delay expression for the short-channel case would still have two factors, a temperature-only-dependent mobility factor [$F(T)$ in (6)] and the rest that depends only on the process variations [$G(P)$ in (6)]. This explains why the one-point calibration simulation with 0.13 μm transistors worked in Section II-B.

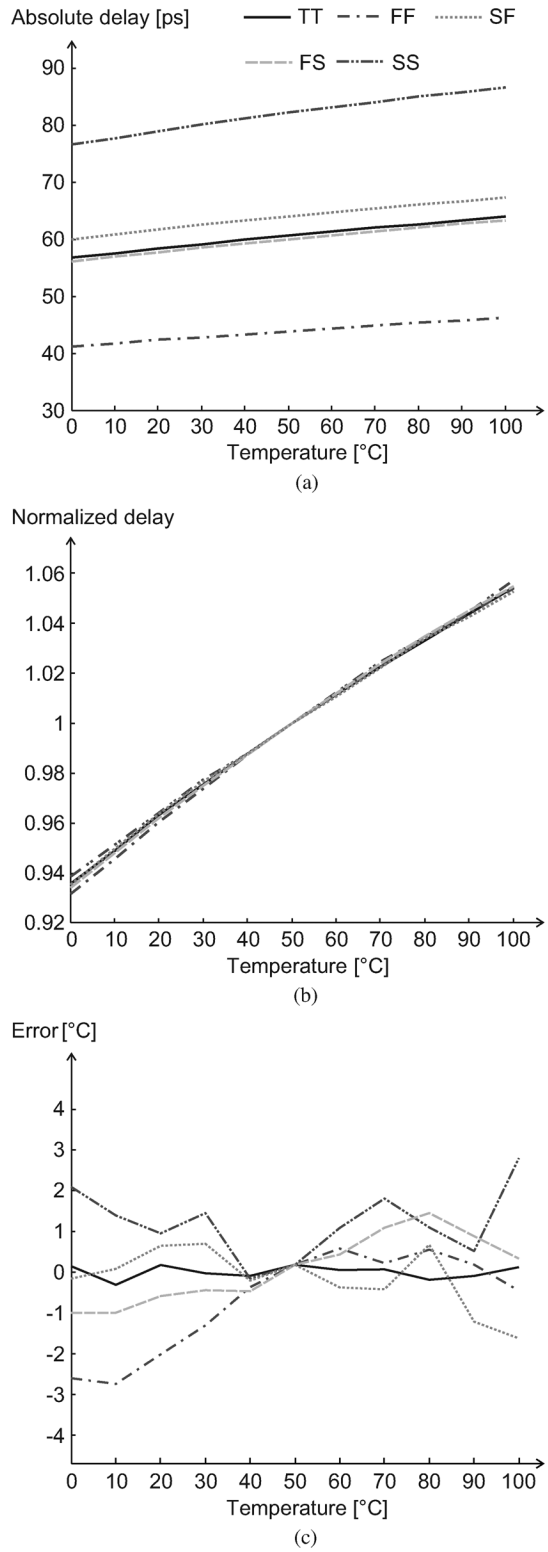

Fig. 2. (a) Simulated absolute delays across all process corners. (b) Normalized delays obtained from the simulated absolute delays. (c) Simulated errors corresponding to small remaining process-to-process variations in the normalized delays. The errors correspond to deviations of the normalized delays from a master curve, extracted from the normalized delays via least square distance fitting.

Note that the separation of variables is possible because the temperature dependency of the threshold voltage does not strongly affect the temperature dependency of the inverter delay. This, however, may not be true in an aggressively scaled

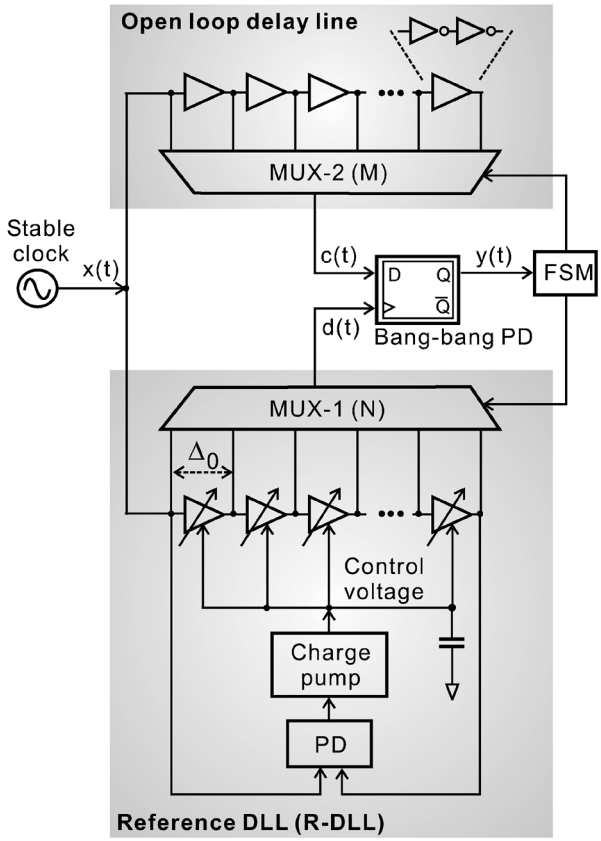

Fig. 3. DLL-based CMOS temperature sensor.

CMOS technology (e.g., tens of nanometers), in which case our approach might be limited or need a modification.

III. Operating Principle (2)—Dual-DLL-Based Delay Measurement

Implementation of the idea of the foregoing section involves measuring the inverter delay at a known temperature T_c, and measuring the delay at an unknown temperature T we seek to find out. Dividing the latter by the former yields the normalized delay, a faithful temperature representation to the first order. We execute this protocol using the DLL-based architecture of Fig. 3, which is a build up from the basic delay-based temperature sensor architecture of Fig. 1(b). Although only one DLL is explicit in Fig. 3, it will shortly become clear that it actually involves two DLLs.

The architecture of Fig. 3 contains an open-loop delay line at the top, whose delay varies with temperature and process variations, and a charge-pump DLL at the bottom, which synthesizes delay references independent of temperature and process variations. This reference-DLL (R-DLL) is locked to a crystal oscillator $x(t)$, thus, each delay cell in the R-DLL has a constant delay, Δ_0, which remains constant despite temperature and process variations. MUX-1 taps a node in the R-DLL's delay line to produce R-DLL output $d(t)$: if Nth cell's output is tapped, the delay between input $x(t)$ and output $d(t)$ of the R-DLL is given by

$$D_{\rm DLL} = N \cdot \Delta_0. \tag{10}$$

This is our delay reference independent of temperature and process variation. N can be altered to produce different delay reference values.

For the open-loop delay line, if Mth cell's output is tapped by MUX-2, the delay between input $x(t)$ and output $c(t)$ of the open-loop line at temperature T becomes

$$D_{OL}(T,P) = F(T) \cdot M \cdot G(P) \tag{11}$$

where we have multiplied (6) by M. This delay varies with both temperature and process variation.

Now we explain how the architecture of Fig. 3 measures temperature with one-point calibration of Section II.

A. Calibration Mode

In calibration mode, temperature is set at a known value, T_c, and the MUX-1 setting, N, is set at a constant, N_c, to fix the R-DLL's reference delay at $D_{\rm DLL} = N_c\Delta_0$. We then increase M (MUX-2 setting) until the open-loop line's delay D_{OL} equals the fixed reference delay, $D_{\rm DLL} = N_c\Delta_0$, at $M = M_c$. The comparison of D_{OL} to $D_{\rm DLL}$ to find their "lock" at $M = M_c$ is done via the bang-bang phase detector in Fig. 3. In this sense, the entire architecture of Fig. 3 may be viewed as another DLL, which we call measuring DLL (M-DLL). This perspective and the process of finding $M = M_c$ are captured in Fig. 4(a). At $M = M_c$, we have the following *calibration equation*

$$F(T_c) \cdot M_c \cdot G(P) = N_c. \cdot \Delta_0. \tag{12}$$

Since the right hand side and $F(T_c)$ are constants, $M_c \cdot G(P)$ is constant across all process corners: if $G(P)$ is smaller, a larger M_c is chosen; if $G(P)$ is larger, a smaller M_c is chosen. It is the constant product $M_c \cdot G(P)$ obtained in this calibration stage that is used later in the measurement mode to compensate for process variation. This is the end of calibration (which, in practice, would be done in production line). MUX-2 now has a hardwired setting, $M = M_c$.

B. Measurement Mode

After the one-point calibration at T_c, the sensor enters a mode where it measures its ambient temperature T. As T is unknown, D_{OL} of the hardwired open-loop line with $M = M_c$ is an unknown delay. The M-DLL measures D_{OL} by varying the reference delay $D_{\rm DLL}$ of the R-DLL, as in Fig. 4(b): MUX-1 setting N is increased until $D_{\rm DLL}$ equals D_{OL} at $N = N_m$ (subscript "m" denotes "measurement"). At this point, we have the following *measurement equation*:

$$F(T) \cdot M_c \cdot G(P) = N_m \cdot \Delta_0. \tag{13}$$

N_m is a function of temperature only, independent of the process variations. This can be seen by eliminating the product $M_c \cdot G(P)$, which was fixed at a constant value in the calibration mode, in (13) using (12)

$$N_m = \frac{F(T)}{F(T_c)} \cdot N_c = \left(\frac{T_c}{T}\right)^{\alpha} \cdot N_c. \tag{14}$$

As can be seen, N_m is a digital output that accurately (to the first order) represents temperature T, unaffected by the process variation. The effect of the process variation has been removed by the one-point calibration that fixed $M_c \cdot G(P)$ at a constant

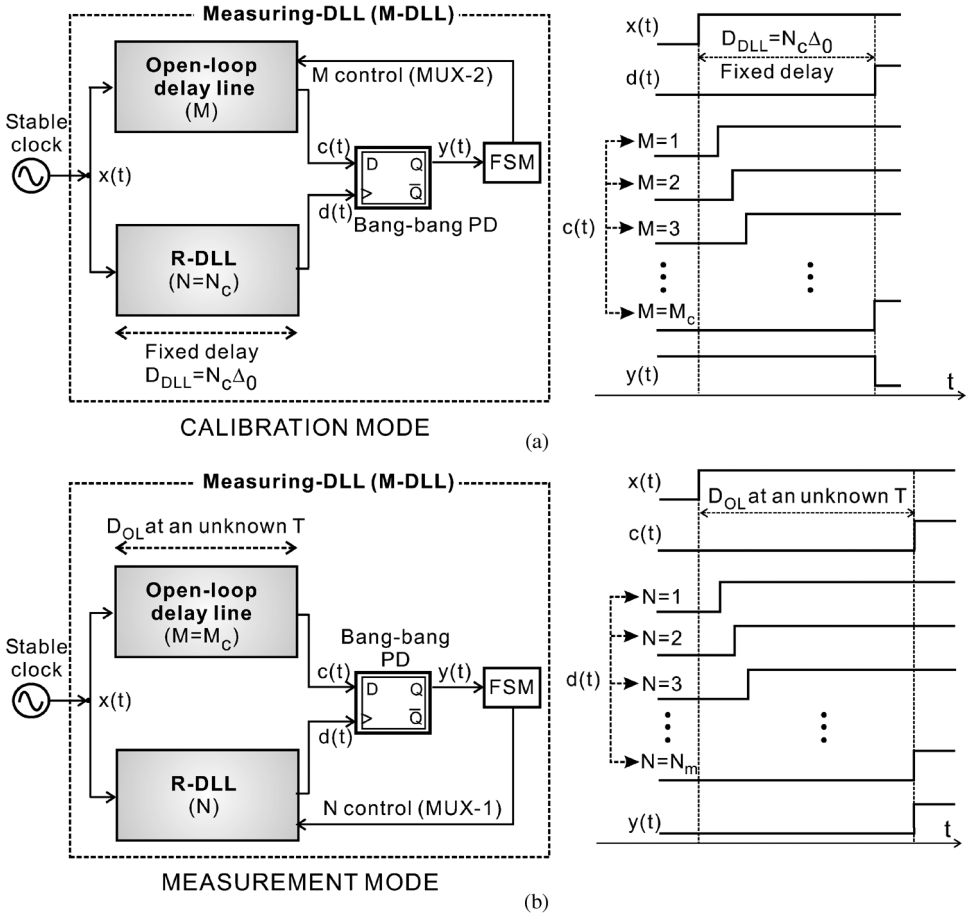

Fig. 4. (a) Calibration mode. When M is small, the rising edge of $c(t)$ leads that of $d(t)$. With increasing M, the former approaches the latter. When the former eventually lags the latter with $M = M_c$, the bang-bang phase detector output $y(t)$ changes from one to zero, which is detected by the finite state machine to store M_c. (b) Measurement mode. The operation is the same as the calibration mode, while N is now increased with $M = M_c$.

value. Equation (14) corresponds to the normalized delay of (9). Note that the calibration and measurement operation with Fig. 3 naturally includes the delay normalization: all we need is to read out the digital output N_m as a process-independent representation of temperature.

IV. Design and Implementation

The implemented sensor is schematically shown in Fig. 5, which is a detailed version of Fig. 3. The R-DLL, shown in the lower portion, consists of a voltage-controlled delay line (VCDL), a phase detector, and a charge-pump in a closed loop. The VCDL is an even-numbered cascade of current-starved inverters. The open-loop delay line, at top of Fig. 5, is an even-numbered cascade of CMOS inverters. The R-DLL is locked to a 30 MHz stable clock $x(t)$, which also drives the open-loop delay line. The period P_0 of $x(t)$ is $P_0 \approx 33.3$ ns.

In the R-DLL (see Fig. 5), the VCDL contains a total of 200 delay buffers. 32 of them (164th $\sim$ 195th) are connected to MUX-1. The input and output phases of a buffer selected by MUX-1 serve as two input phases for the tristate-inverter-based phase interpolator [34], [35] consisting of 16 inverters. One of the two phases from MUX-1 is tapped to the inputs of 8 inverters; the other phase from MUX-1 is tapped to the inputs of the remaining 8 inverters. The 16 inverters are all tied at output. A 16-bit control input (an 8-bit enable signal and its negation) turns on only 8 inverters proper. By varying the combination of the 8 inverters that are turned on, the output phase can be interpolated at 7 different positions between the two input phases. In this way, the interpolator generates 7 additional phases between its two input phases. This arrangement is to achieve a measurement range of $0 \sim 100\,^{\circ}\mathrm{C}$ and a sub-$^{\circ}\mathrm{C}$ measurement resolution.

A. Temperature Range

In calibration mode ($T = T_c$), MUX-1 selects the N_cth buffer in the R-DLL ($N_c = 164 \sim 195$; specific choice of N_c is variable) to fix the reference delay, D_{DLL}. Since the delay through the entire 200 buffers of the R-DLL is P_0, $D_{\mathrm{DLL}} = P_0 \cdot N_c/200$ (here we assume no phase interpolator, which is to acquire the target resolution, as will be discussed shortly). At the end of the calibration, $D_{OL} = D_{\mathrm{DLL}} = P_0 \cdot N_c/200$.

In measurement mode, D_{OL} deviates from $P_0 \cdot N_c/200$ as temperature is not T_c any more. Simulations indicate that D_{OL} varies by ca. 10% as temperature varies from 0 to 100 °C, i.e., $\Delta D_{OL} \approx P_0 \cdot N_c/2000$ for $\Delta T = 100\,^{\circ}\mathrm{C}$. The maximum ΔD_{OL} is 3.22 ns for $N_c = 195$. This variation of D_{OL} is measured using the R-DLL. Since 32 buffers in the R-DLL are connected to MUX-1, the R-DLL's delay can be varied maximally by $P_0 \cdot 32/200 = 5.28$ ns. This is larger than the aforementioned 3.22 ns, thus, the temperature measurement range of $0 \sim 100\,^{\circ}\mathrm{C}$ is covered.

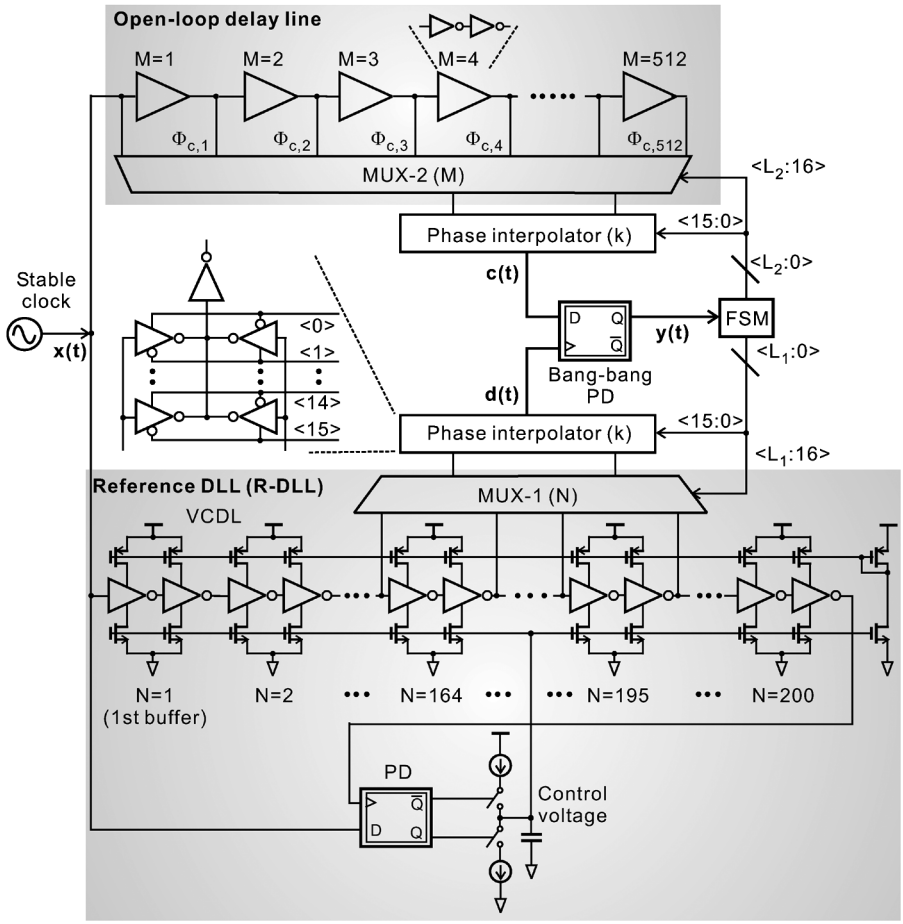

Fig. 5. Detailed schematic of the DLL-based CMOS temperature sensor.

B. Temperature Resolution

To attain a sub-°C measurement resolution, consider mapping $\Delta D_{OL} = 3.22$ ns for $\Delta T = 100\,^{\circ}\mathrm{C}$ to a 7-bit digital output. For this, D_{DLL} should be able to vary with a step of 3.22 ns/$2^7 = 25$ ps. Since the minimum achievable delay by a single buffer is only about 100 ps, we are to improve the time resolution of the R-DLL. The phase interpolator [34], [35] achieves the fine resolution, by generating additional 7 phases. Owed to this interpolator, the time resolution of the R-DLL, which is given by $P_0/200/8$, becomes 20 ps, with which we can attain the 7-bit resolution.

C. Calibration and Measurement Algorithm

Owed to the phase interpolators, the calibration and measurement algorithm of Section III can be improved, albeit of the same essence, to have finer time resolution. Let us consider, as an example, the calibration mode, with reference to Figs. 5 and 6. In the calibration mode, D_{DLL} is held constant by fixing the R-DLL's buffer index N and its phase interpolator index k. The open-loop delay line consists of a total of 512 buffers (indexed as $M = 1 \sim 512$), all connected to MUX-2. The goal of the calibration mode is to identify, for the open-loop delay line, the specific buffer index M and interpolator index k, with which $D_{OL} = D_{\mathrm{DLL}}$. We first find M (coarse search), then k (fine search).

In the beginning of the coarse search, $M = 1$ and $k = 8$ (the interpolator selects $\Phi_{c,1}$, the output of the 1st buffer, as its output

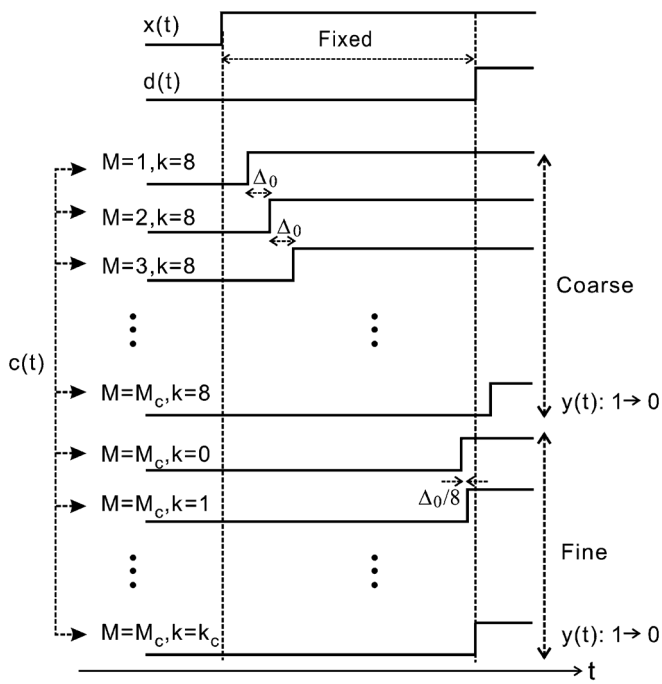

Fig. 6. Calibration algorithm in the presence of the phase interpolator.

phase). M is then increased one by one with $k = 8$ maintained, until the bang-bang phase detector senses the rising edge of $c(t)$ after the rising edge of $d(t)$ at $M = M_c$ (see Fig. 6). The M_cth buffer has been chosen for the open-loop delay line. Now with

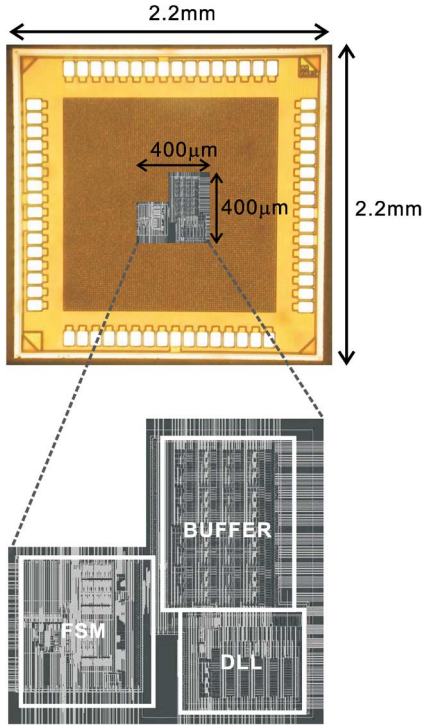

Fig. 7. Die micrograph.

this buffer, k is increased one by one from 0 for the fine search, until the bang-bang phase detector once again senses the rising edge of $c(t)$ after the rising edge of $d(t)$ at $k = k_c$ (see Fig. 6). We have found $M = M_c$ and $k = k_c$, and D_{OL} has been made equal to the fixed $D_{\rm DLL}$ within the given resolution. The measurement mode works exactly the same way: at the end of a measurement, N_m and k_m for the R-DLL are determined.

In the absence of phase interpolators, $D_{\rm DLL}$ was given by $N\Delta_0$, where N is MUX-1 setting. With the phase interpolator, $D_{\rm DLL}$ is given by $\{8(N-1)+k\}\Delta_0/8$, where N is MUX-1 setting and k is the phase interpolator index. We take $\{8(N-1)+k\}$ as the digital representation, N', of $D_{\rm DLL}$

$$N' \equiv 8(N-1)+k. \tag{15}$$

Likewise, the digital representation, M', of D_{OL}, is taken as

$$M' \equiv 8(M-1)+k. \tag{16}$$

V. Measurements

The temperature sensors were fabricated in 0.13-μm digital CMOS. Fig. 7 shows a die micrograph. As metal fills block the view of the active area, its physical layout is shown where it lies. The active area of the pad-limited chip is 0.12 mm^2.

A total of 15 chips were measured. Each tested die was placed in a 9-mm MLF 64-pin package, which was inserted into a Plastronics 64-pin MLF socket. The socket was mounted on a printed circuit board. A 1.2 V supply was used. A 30 MHz clock signal ($x(t)$, Fig. 5) is produced by an Agilent 33250A function generator. A National Instrument PCIe-6536 I/O card was used to collect digital outputs. An Envirotronics EnviroFLX500 temperature chamber with control accuracy of $\pm 1.1\,^\circ$C was used for temperature control.

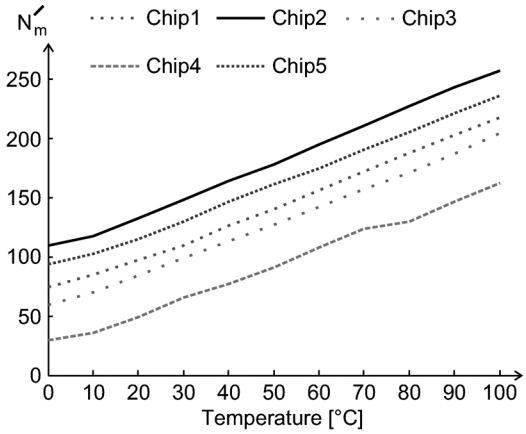

Fig. 8. Measurements with no proper calibration.

A. Measurements With no Proper Calibration

We first show the consequence of lack of proper calibration. For this task, we measured only 5 chips, which is sufficient to show the essence. First, one chip was selected and one-point calibration was performed at $T_c = 50\,^\circ$C with a fixed R-DLL reference delay index of $N'_c = 140 (N_c = 18, k = 4)$ [see (15)].[2] M'_c is obtained as a result of the one-point calibration for the selected chip. M' in each of the 5 chips was fixed at this same M'_c. In other words, only the selected chip was calibrated, while none of the remaining 4 chips was calibrated according to their own process variations. Subsequently, the R-DLL delay index N'_m was measured for each of the 5 chips, at temperatures from 0 to 100 °C with a step of 10 °C. Fig. 8 shows the results. Due to the lack of proper calibration, N'_m-versus-T curves are not consistent amongst different chips.

B. Measurements With Proper Calibration

The next set of measurements were done for a total of 15 chips with proper calibration. One-point calibration was performed for each chip, according to its own process variation, and as a result of calibration, each chip is assigned with its own M'_c value. After these calibrations, N'_m-versus-T was measured for each chip. The 15 N'_m-versus-T curves are shown altogether in Fig. 9: as compared to Fig. 8, the curves are more consistent across the 15 chips, and chip-to-chip process variations have been largely removed, which validates the one-point calibration.

Smaller chip-to-chip variations remain in the N'_m-versus-T curves of Fig. 9. To quantify the corresponding error, we first obtain a master curve from the N'_m-versus-T curves via a third-order fitting. Deviations of the N'_m-versus-T curves from the master curve correspond to an error of $-4.0 \sim 4.0\,^\circ$C in the range of $0 \sim 100\,^\circ$C (see Fig. 10). Part of this error is caused by the aforementioned control uncertainty of $\pm 1.1\,^\circ$C of the temperature chamber used [this control uncertainty also accounts for the non-zero error at the calibration temperature 50 °C (see Fig. 10)]. The remaining error, after factoring out the chamber's control uncertainty, represents the fundamental sensor error caused by the approximate nature of the one-point

[2] N_c actually corresponds to the 18th buffer from the 164th buffer in the R-DLL's VCDL (see Fig. 5), thus, the real N_c is 181 and the real N'_c is 1444. Here and in what follows, we use this re-scaled index scheme for N and N'.

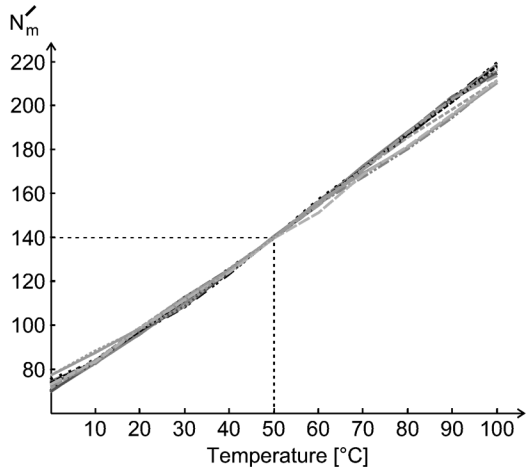

Fig. 9. Measurements of 15 chips after proper calibration for each chip.

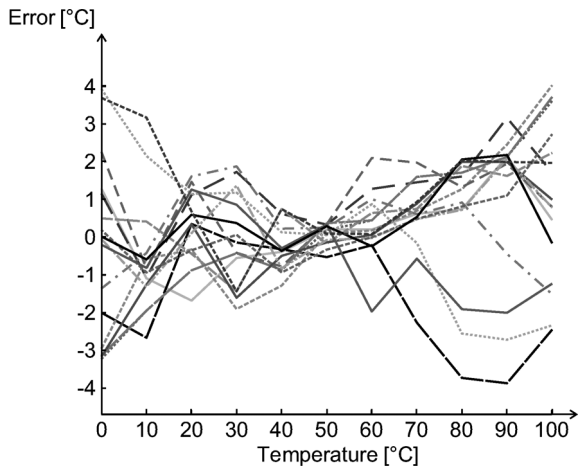

Fig. 10. Temperature measurement errors for the 15 chips.

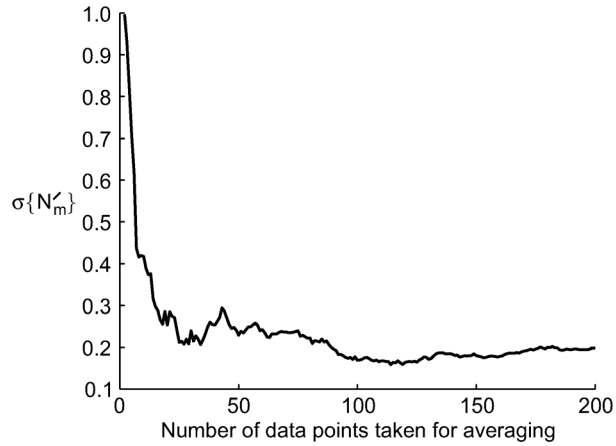

Fig. 11. Standard deviation of averaged N'_m at $T = 30\,^{\circ}\mathrm{C}$ in Chip 1 as a function of the number of data points taken for averaging.

calibration (see Section II). The measurement resolution obtained from the master curve is around 0.66 °C per LSB for 7-bit digital outputs.

The comparison of our sensor to the prior delay-based sensors is provided in Section V-D, after presenting the measurement bandwidth and energy of our sensor in the following subsection.

C. Data Averaging and Measurement Bandwidth

Jitters (e.g., in the R-DLL) and ac variations of supply cause fluctuations in the digital outputs. To minimize resultant errors, the digital outputs can be averaged. Each reported N'_m in the foregoing subsections is indeed an averaged value: for a given temperature, a single measurement was done at every 2 μs, and 100 such single measurements were averaged using an external computer to obtain each of the averaged digital output, N'_m.

We average 100 measurements for the following reason. As more data are averaged, fluctuations are suppressed more, tending towards a more accurate measurement. This tendency is evident in Fig. 11, where the standard deviation of averaged N'_m in one chip at one example temperature is shown as a function of the number of measurements taken for averaging. Fig. 11 also shows that averaging more than 100 data will not reduce the error any further (possibly due to time-correlation of the fluctuations). Thus to minimize the fluctuation error while not wasting unnecessary energy, we chose 100 data points for averaging.

Since a single measurement is done at the rate of 500 kHz, with the averaging of 100 measurements, the effective sampling rate (the rate of obtaining one averaged digital output N'_m) is 5 kilo-samples/s. Since the power dissipation of the sensor[3] is 1.2 mW, the energy used to obtain one averaged digital output is 0.24 μJ. The large measurement bandwidth, with which fast thermal transients can be tracked, and the low energy per averaged sample, are attributed to the DLL-based operation of our sensor.

For one-point calibration which also involves data averaging, it takes 0.5 ms to obtain an averaged M'_c. In practice, this calibration (including the averaging) is performed only once at production line.

D. Performance Comparison to Prior Delay-Based Sensors

Table I compares this work to delay-based temperature sensors with two-point calibration [18]–[22]. For completeness, the table also includes delay-based temperature sensors with one-point calibration [23], [24], which appeared after the present work was originally reported in [25].

First, our sensor tends towards a larger error than other works, e.g., [18]–[22] with two-point calibration, which is due to the one-point calibration we use. Nonetheless, our accuracy is deemed sufficient for microprocessor thermal profiling [5], [6], [31]–[33]. Additionally, the one-point calibration has the advantage of simplicity and low-cost, which is a desirable feature in the microprocessor application (see Sections I and II).

Second, our sensor using the dual-DLL architecture with multiple delay references achieve a high bandwidth of 5 kilo-samples/s, as we compare the effective sampling rates of the sensors at which errors were actually measured.

[3]In practice with on-chip averaging, power consumed for averaging must be considered. On-chip averaging can be done with a digital filter with a bandwidth of 500 kHz (measurement rate). We expect the associated power dissipation to be far less than the 1.2 mW.

TABLE I
COMPARISON TO OTHER DELAY-BASED TEMPERATURE SENSORS

	# of Calibration Points	Range (°C)	Error (°C)	Energy (μJ/sample)	Conversion Rate[a] (samples/s)	Resolution (°C)	Area (mm^2)	CMOS Process (μm)
This Work	1	0∼100	−4.0∼4.0[b]	0.24	5k	0.78	0.12	0.13
[18]	2	0∼100	−0.7∼0.9	5	2	0.16	0.175	0.35
[19]	2	−40∼95	−0.8∼0.8	0.45	20	0.523	0.4	0.35
[20]	2	0∼75	−1.5∼0.8	4.2	2	0.058	N/A (FPGA)	FPGA
[21]	2	−40∼60	−0.6∼0.6	0.3	5	0.09	0.09	0.35
[22]	2	0∼90	−0.25∼0.35	18	2	0.09	0.6	0.35
[23][c]	1	0∼100	−0.7∼0.6	0.18	1	0.133	N/A (FPGA)	FPGA
[24][c]	1	−40∼110	−2.7∼2.9	0.0011	366k	0.043	0.0066	0.065

[a] The conversion rates cited are the ones at which the error measurements were done.

[b] With temperature chamber's control uncertainty of ±1.1 °C.

[c] These one-point calibration works appeared after the present work was originally reported in [25].

VI. SENSITIVITY TO STATIC SUPPLY SHIFT—MEASUREMENT AND ANALYSIS

Delay-based CMOS temperature sensors [18]–[24] are prone to high sensitivity to static power supply shift. Our design in this paper does not overcome this issue either. Before concluding this paper, we discuss this problem with explicit measurements of the sensitivity of our sensor to static supply shift, so as to motivate further studies.

When CMOS inverters are used for the open-loop delay line as in this work and [18]–[22], its delay depends directly on $V_{\rm dd}$ [e.g., (1)]. Therefore, a static difference of $V_{\rm dd}$ between calibration and measurement can cause large measurement errors (ac fluctuations of $V_{\rm dd}$ are averaged out, as seen earlier). A static shift in $V_{\rm dd}$ occurs when, for instance, the IR drops are different between calibration in production line and measurement at user end.

$V_{\rm dd}$'s static shift causes measurement errors as follows. The $V_{\rm dd}$-dependence of CMOS inverter's delay is captured entirely by the $V_{\rm dd}$-dependence of $G(P)$ in (5). Therefore we rewrite $G(P)$ as $G(P, V_{\rm dd})$. If $V_{\rm dd}$ is the same between calibration and measurement, the normalized delay formula, (9), holds true, and the sensor operates in the way it has been described. Indeed, all measurements in the foregoing subsections were done after ensuring, using an off-chip voltage regulator, $V_{\rm dd}$ to remain constant to the third significant digit between calibration and measurement. In contrast, if there is a static shift in $V_{\rm dd}$ between measurement and calibration, the normalized delay formula of (9) is altered to

$$D_{\rm norm} = \left(\frac{T_c}{T}\right)^{\alpha} \cdot \frac{G(P, V_{{\rm dd},m})}{G(P, V_{{\rm dd},c})} \tag{17}$$

where $V_{{\rm dd},m}$ and $V_{{\rm dd},c}$ are supplies for measurement and calibration. The G-functions do not cancel, and the normalized delay does not faithfully represent temperature any more.

To measure the impact of the static $V_{\rm dd}$ shift, we first calibrate a sensor IC at $T = 50\,^{\circ}$C with $N'_c = 120$ and $V_{\rm dd} = 1.200$ V.

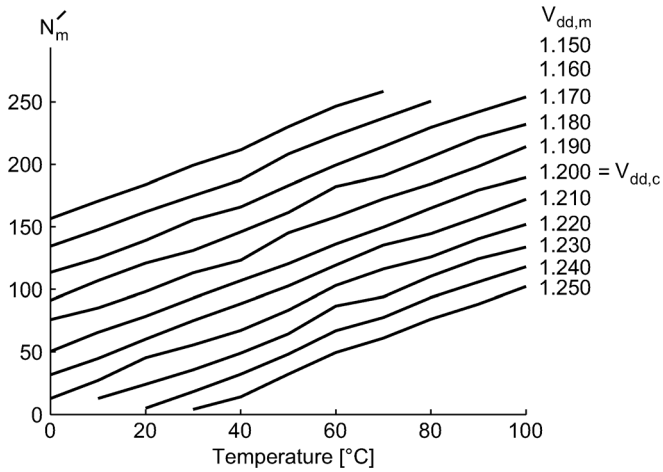

Fig. 12. Temperature measurement using a sensor chip after calibration. Supply voltage is varied from the calibration supply of 1.200 V.

We then measure N'_m for T from 0 to 100 °C, also varying $V_{\rm dd}$ with a step of 10 mV around 1.200 V. The results are in Fig. 12. Different N'_m-versus-T curves result, as $V_{\rm dd}$ is altered. Thus, a change in N'_m due to a $V_{\rm dd}$ shift for a fixed T can be misunderstood as a T change. We now quantify this error caused by the static $V_{\rm dd}$ shift.

The normalized delay is a function of T and $V_{\rm dd}$: in (17), $V_{{\rm dd},c}$ is a constant, while $V_{{\rm dd},m}$ is the variable we have just denoted as $V_{\rm dd}$. The process variation P is not considered here, as it remains the same in a given chip. The variation of the normalized delay, $\Delta D_{\rm norm}$, due to a small temperature change ΔT with a fixed $V_{\rm dd}$ is given by

$$\Delta D_{\rm norm} = \frac{\partial D_{\rm norm}}{\partial T} \Delta T. \tag{18}$$

Similarly, $\Delta D_{\rm norm}$ due to a small supply shift $\Delta V_{\rm dd}$ with a fixed T is given by

$$\Delta D_{\rm norm} = \frac{\partial D_{\rm norm}}{\partial V_{\rm dd}} \Delta V_{\rm dd}. \tag{19}$$

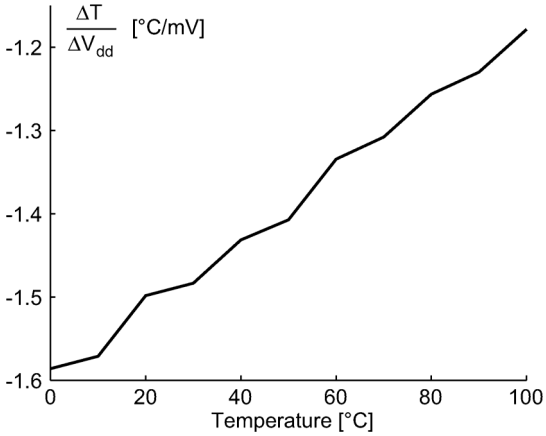

Fig. 13. $\Delta T/ = \Delta V_{\rm dd}$ versus T around $V_{\rm dd} = 1.200$ V.

Therefore, ΔT with a fixed $V_{\rm dd}$ and $\Delta V_{\rm dd}$ with a fixed T would yield the same $\Delta D_{\rm norm}$, if ΔT and $\Delta V_{\rm dd}$ satisfied the following relation:

$$\frac{\Delta T}{\Delta V_{\rm dd}} = \frac{\partial D_{\rm norm}}{\partial V_{\rm dd}} \Big/ \frac{\partial D_{\rm norm}}{\partial T}. \tag{20}$$

Using $\partial D_{\rm norm}/\partial V_{\rm dd}$ and $\partial D_{\rm norm}/\partial T$ extracted from Fig. 12, we plot $\Delta T/\Delta V_{\rm dd}$ as a function of T in Fig. 13. $|\Delta T/\Delta V_{\rm dd}|$ is as large as 1.6 °C/mV, i.e., a 1 mV of $V_{\rm dd}$ shift can be misconceived as a 1.6 °C of temperature change. Hence, our current implementation (and all other delay-based sensors using CMOS inverters as delay elements [18]–[24]) can yield significant errors in the presence of supply shift.

This problem can be potentially solved: 1) by adding a local voltage regulator proximate to the sensor so that $V_{\rm dd}$ is maintained at the same level between calibration and measurement or 2) by using an open-loop delay line consisting of current-starved inverters, whose delay can be made sensitive to temperature, but much less sensitive to $V_{\rm dd}$ [36]. Actual design and experimental verification are open to future work.

VII. Conclusion

The recent temperature sensor work in [18]–[22] exploits the temperature dependence of CMOS inverter delays. The work of this paper is an expansion of, and a departure from, the prior delay-based sensor works. The following two main contributions are: 1) operation of the delay-based sensor with simple and low-cost one-point calibration and 2) new architecture using DLLs that enhance measurement bandwidth for fast thermal monitoring. This CMOS temperature sensor with low energy per sample (0.24 μJ/sample), a high conversion rate (5 kilosamples/s), and calibration simplicity may be potentially well suited for microprocessor thermal management applications. Its high sensitivity to a static supply shift remains as a problem to address.

Acknowledgment

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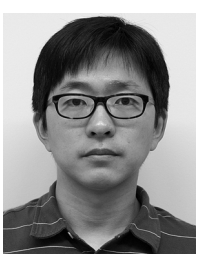

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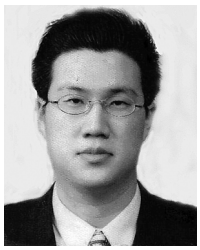

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