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SUPPLEMENTARY INFORMATION

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CMOS nanoelectrode array for all-electrical intracellular electrophysiological imaging

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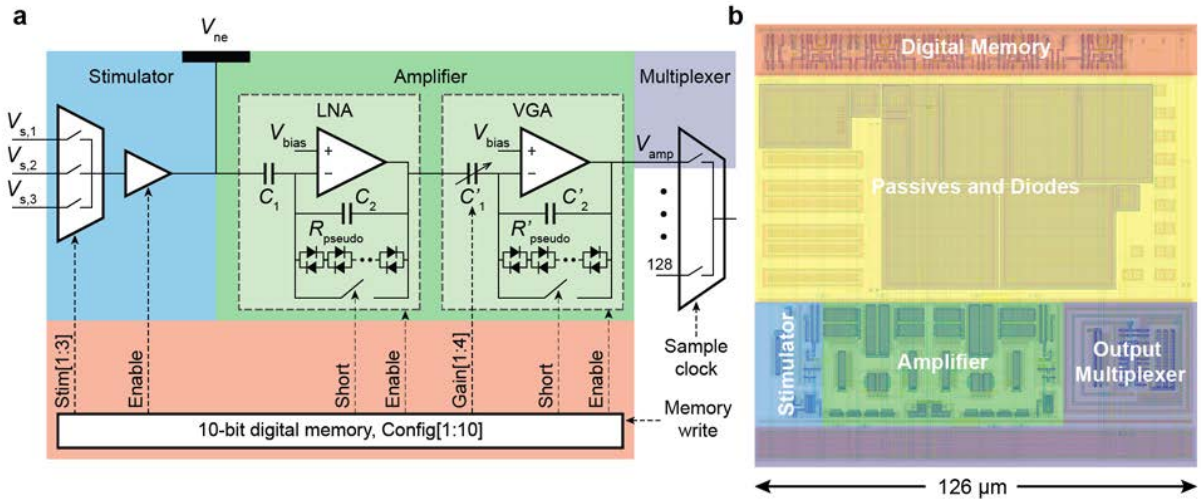
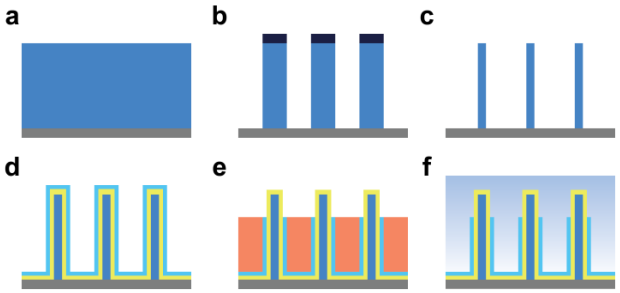
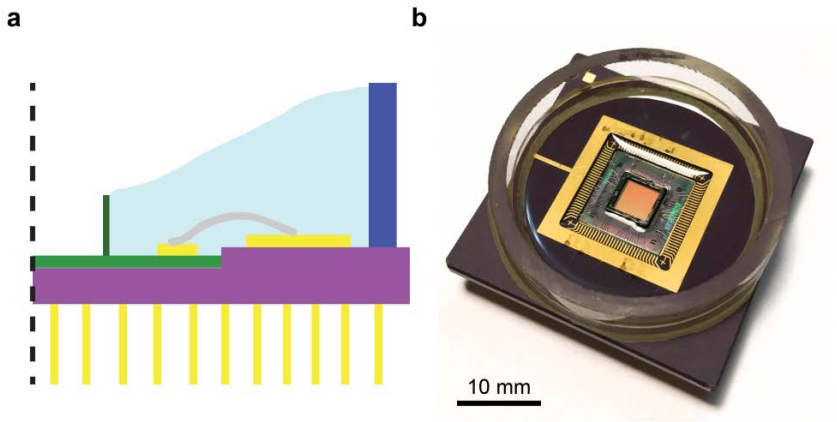


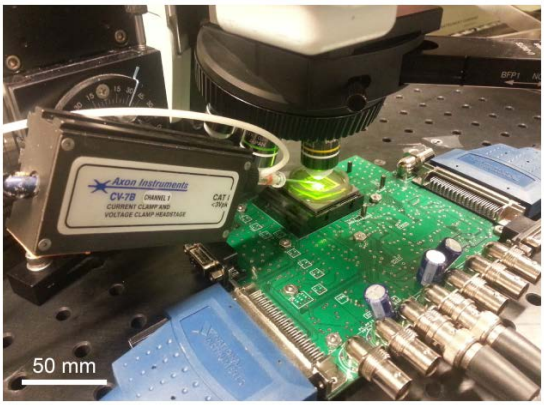
Supplementary Figure 1 | Schematic and physical layout of the CMOS pixel circuit. a, The three major building blocks of the CMOS pixel circuit are a 10-bit digital memory, a stimulator accompanied by a 3:1 input MUX, and an amplifier consisting of a low noise amplifier (LNA) followed by a variable gain amplifier (VGA). Each pixel also includes a single input of a 128:1 output multiplexer and a metallic pad in which nanoelectrodes are post fabricated. **b,** The pixel layout of these building blocks is from the computer aided design (CAD) software (Cadence) due to the underlying structures being difficult to image in the actual IC. The figure separately shows important passive components, such as an on-chip blocking capacitor at the amplifier input, and *pn* junction diodes in the amplifier feedback paths.



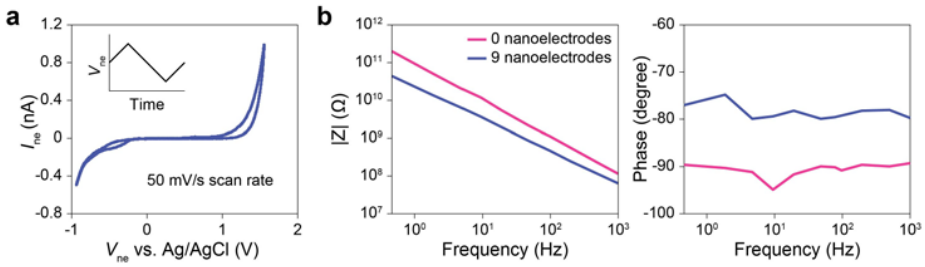
Supplementary Figure 2 | Process flow for vertical nanoelectrode fabrication. a, A 3-µm thick SiO_2 layer is deposited on the pixel pad using plasma-enhanced chemical vapor deposition (PECVD). **b,** Stepper lithography and dry etching defines a 1-µm diameter vertical SiO_2 pillar. **c,** Further wet etching creates narrow SiO_2 pillars of ~100-nm diameter to form the core support for the nanoelectrodes. **d,** 5-nm thick Ti and 20-nm thick Pt are sputtered on to SiO_2 pillars to form a conductive coating of the nanoelectrodes. An additional 20-nm thick SiO_2 passivation layer is deposited using atomic layer deposition (ALD). **e,** A spin-coated thin resist is used to protect the base insulation while a wet etch is used to expose the metal tip. **f,** Finished nanoelectrodes: the exposed metal tip in solution allows for electrical interrogation while the pillar base and the pad are insulated with SiO_2 to form a tight seal to cellular membranes.



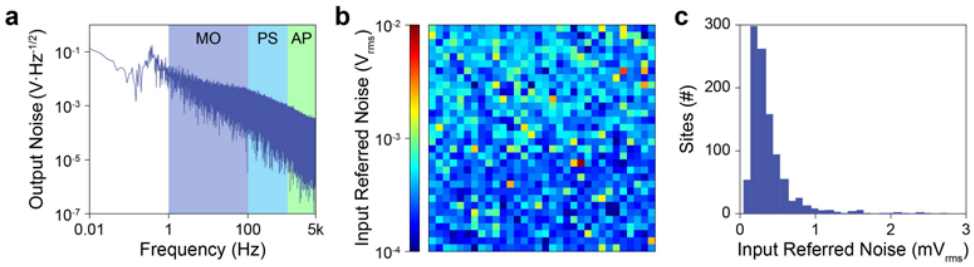
Supplementary Figure 3 | Packaging of CNEA device. a, The CNEA chip (green and gold) is attached and wire-bonded (grey) to a pin grid array chip carrier (purple and gold), obtained from Spectrum Semiconductor Material (San Jose, CA). A ~4 mm square inner silicon ring (dark green) is epoxied (MasterBond, Hackensack, NJ) in between the inner array and the wire-bonds, and a glass outer ring (dark blue) (Bioptechs, Butler, PA) is epoxied to the chip carrier. Polydimethylsiloxane (PDMS) (light blue) is poured in between the inner and outer rings to encapsulate the bonding wires and to form a well. **b,** Fully packaged CNEA device.



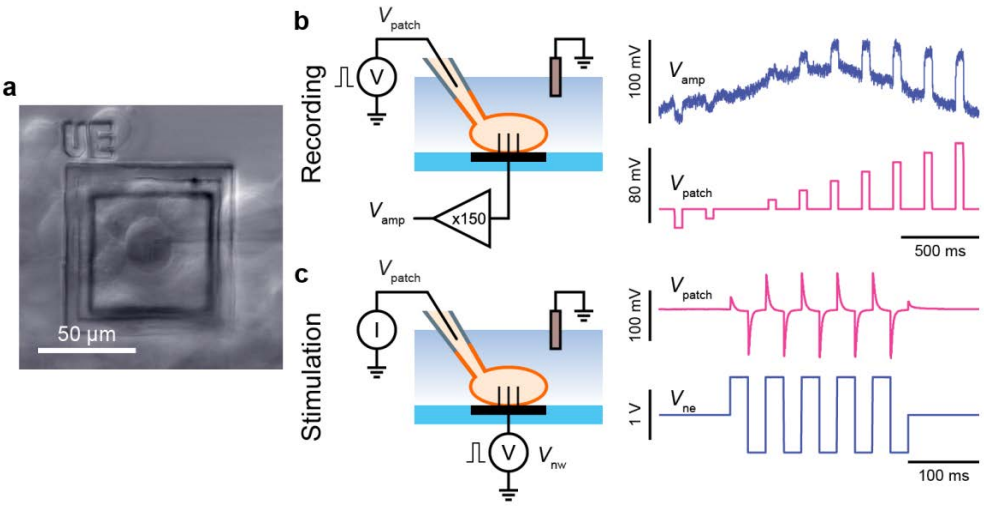
Supplementary Figure 4 | Electrophysiology experimental apparatus. The packaged CNEA device is inserted into a custom designed printed circuit board that interfaces to a computer using a National Instruments data acquisition card. The 8×, 128:1 on-chip analog output multiplexers are digitized at 16-bit resolution and sampled at 1.248 MHz for a total data rate of 20 MB/s. The setup accommodates a patch pipette (left) and fluorescent microscope (top center) for concurrent patch-clamp measurement or fluorescent imaging.



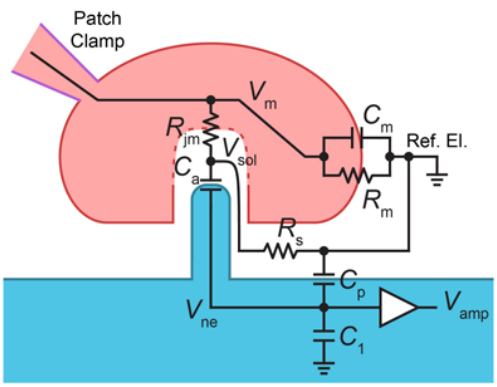
Supplementary Figure 5 | Impedance measurement of the nanoelectrodes in solution. a, Cyclic voltammetry of nine Pt nanoelectrodes in extracellular solution at a scan rate of 50 mV/s . **b,** Electrochemical impedance spectroscopy of a pixel without nanoelectrodes (for measurement of parasitic pad capacitance) and a pixel with nine Pt nanoelectrodes in extracellular solution using a 100 mV amplitude sine wave in the capacitive region.



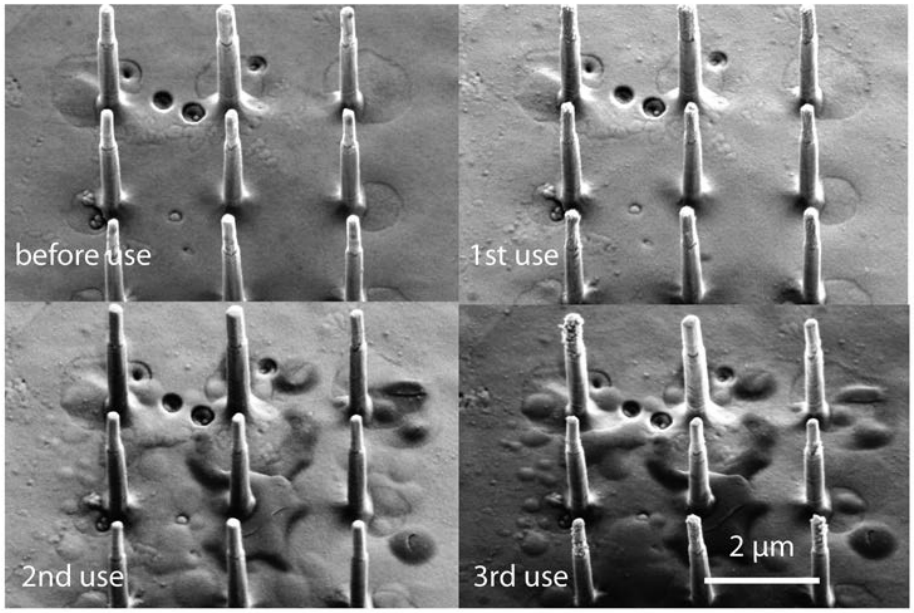
Supplementary Figure 6 | Voltage noise of the pixel amplifier. a, Output voltage noise of a typical amplifier. **b,** Heat map of amplifier input referred noise across the array. **c,** Histogram of input referred noise with a 0.1 mV bin (2 outliers about 3 mV_{rms} omitted).



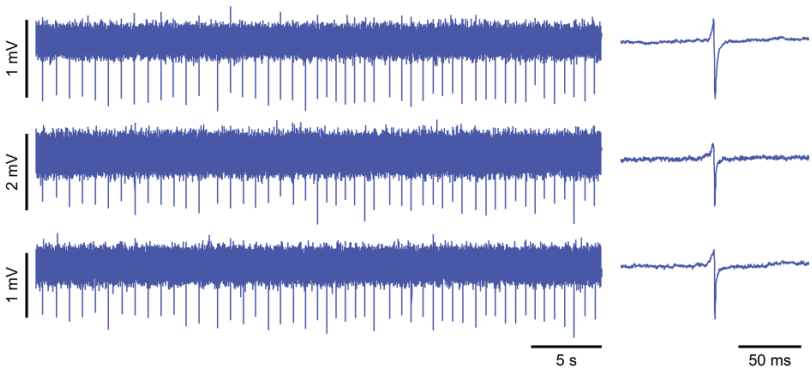
Supplementary Figure 7 | Verification of the CNEA pixel functionality using *in vitro* HEK293 cells. a, Differential interference contrast image showing HEK 293 cells cultured on top of the CNEA chip. The cell on top of the nanoelectrodes is whole-cell patched at the same time. **b,** After the cell was patched and pixel electroporation was performed, the pipette in voltage-clamp mode applied voltage pulses (V_{patch}) with increasing amplitudes to the cell membrane, which were recorded by the CNEA pixel (V_{amp}). The preservation of the waveform shape confirms intracellular access and a linear, flat-band transfer function from the intracellular matrix to amplifier output. The slow oscillation of the amplifier output is due to the low frequency high-pass pole of the bandpass filter configuration of the pixel amplifier. **c,** The pixel stimulator applied biphasic voltage pulses to the nanowires (V_{ne}) and the cell's response was measured by the patch pipette in current-clamp mode (V_{patch}). The transient RC response is due to the nanoelectrode capacitance in series with the intra/extra-cellular solution and membrane resistance.



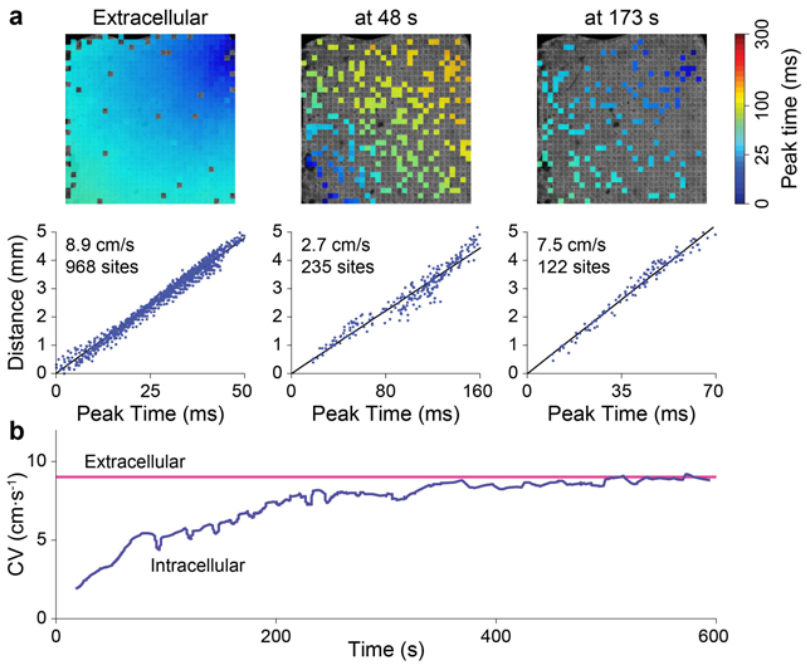
Supplementary Figure 8 | Simplified nanoelectrode-cell small signal equivalent circuit model. A cell sitting on top of a nanoelectrode that is manipulated by a patch clamp pipette in the voltage-clamp mode is modelled by its membrane potential, V_m, membrane capacitance, C_m, and membrane resistance, R_m. The nanoelectrode, biased in the capacitive region, is modelled by an access capacitance, C_a, recording a voltage in solution, V_{sol}, and a parasitic pad capacitance, C_p. The cell-to-electrode interface consists of a porous junctional membrane resistance, R_{jm}, formed by electroporation and a seal resistance, R_s. The CMOS pixel amplifier, amplifying the nanoelectrode voltage, V_{ne}, is simplified to an ideal amplifier with its input impedance, C_1, and output voltage, V_{amp}.



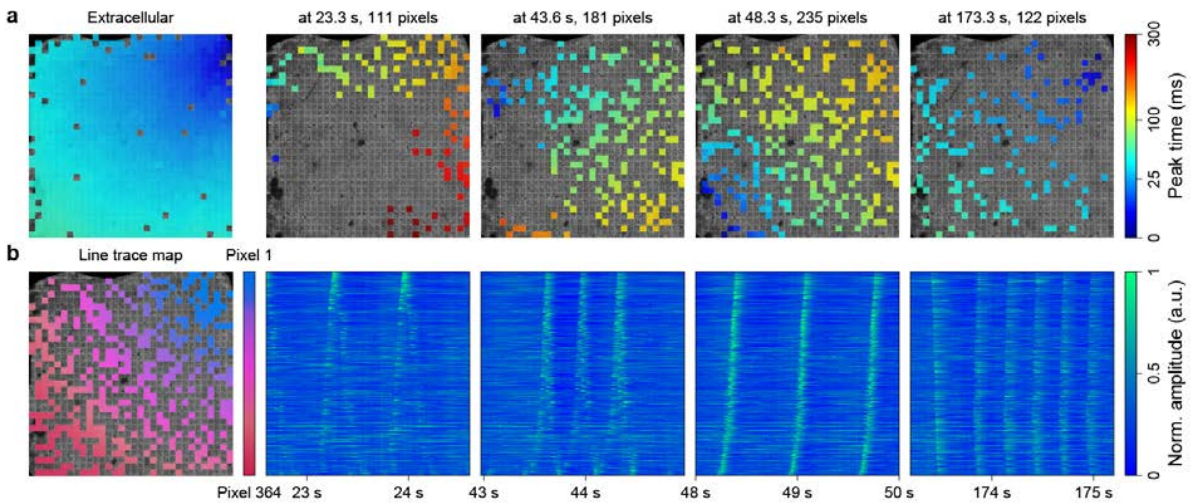
Supplementary Figure 9 | Nanoelectrodes after multiple experiments. SEM images show the integrity of the same nanoelectrodes after multi week-long cultures and electrophysiology experiments.



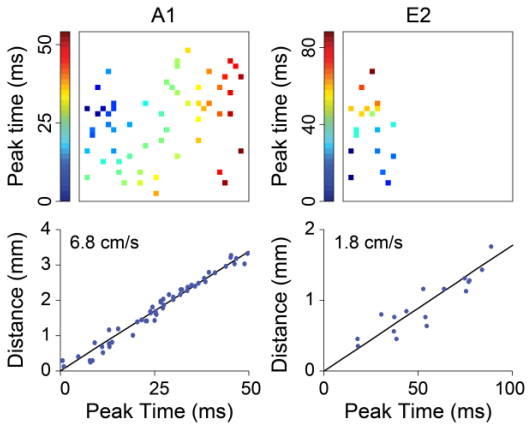
Supplementary Figure 10 | Example recordings of extracellular action potentials of neonatal rat ventricular cardiomyocytes. Extracellular experiments without electroporation were performed on an *in vitro* cardiomyocyte culture; three pixel recordings are shown as examples. The waveforms on the right show the averaged extracellular action potentials for the time period shown on the left.



Supplementary Figure 11 | Conduction velocity (CV) fittings from peak times and CV change with time. a, To calculate CV in the cardiomyocyte sheet in the experiments shown in Fig. 3 of the main text, the peak times from coupled extracellular or intracellular pixels (around at 48 s or 173 s after electroporation) were extracted. The distance of the pixel to the origin of the wave propagation was calculated with the origin swept across the array of the device while performing linear fits using the peak times. The best linear fit, determined from each fit's R^2 value, was used to decide the origin of the wave propagation and to determine the CV. **b,** Similar fittings were performed over the course of the experiment (Figs. 3a & 3b) to calculate CV over time. After electroporation, the CV dropped significantly compared to the extracellularly measured CV before electroporation, and then recovered over time.



Supplementary Figure 12 | Network-level intracellular recording of *in vitro* neonatal rat ventricular cardiomyocyte cultures. a, Repeated from Fig. 3a for convenience, mapping of action potential propagation patterns across the array at different time points before and after electroporation. An extracellular recording before electroporation shows homogeneous action potential propagation, whereas intracellular recordings after electroporation shows an evolution from spiral propagation at 23.3 s and 43.6 s back to homogeneous propagation at 48.3 s and 173.3 s. **b,** Intracellular voltage traces (four right panels) from 364 pixels coupled during the experiment, vertically arranged based on their distance to the upper right corner (see map, left). The amplitude of each pixel is normalized across the four time segments shown. Vertical line slopes represent propagations from lower left. In the first two voltage panels, clockwise spiral propagation is visualized as a change from positive to negative slope. Radially propagating action potentials appear, on the other hand, as single straight lines in the rightmost two panels. The CV, loosely correlated to the slope, is visibly slower at the initial spiral of 23.3 s compared to the later spiral at 43.6 s or the homogeneous propagation at 48.3 s, with the fastest CV at 173.3 s.



Supplementary Figure 13 | CV and propagation map comparison for action potential and EAD propagation. The conduction velocities of action potential A1 and early afterdepolarization (EAD) E2 showed significant difference. In addition, the EAD only propagated in the short APD and transition regions in the leftmost part of the cardiomyocyte sheet.

Supplementary Discussion 1. The design of the CMOS IC

The CMOS IC contains a 32 x 32 pixel array. Supplementary Fig. 1a, which is a detailed version of Fig. 2a of the main text, is a pixel schematic. The pixel includes an amplifier, a stimulator, and a memory, all of which lie underneath the pixel nanoelectrodes. The 10-bit memory (Config[1:10]) enables or disables the amplifier and stimulator (2 bits), thus determining the pixel operation mode between recording and excitation. The memory also controls the electrical characteristics of the amplifier and stimulator. The amplifier is the most challenging pixel component to realize because it processes the weak electrophysiological signals measured by the nanoelectrodes, and thus must achieve adequate gain, noise, and bandwidth. The final design reaches a balance among the amplifier parameters—as discussed shortly—within the pixel area of 126 μm × 126 μm and a maximum pixel power consumption of 12 μW (with amplifier on and stimulator off).

The amplifier consists of a low noise amplifier (LNA) followed by a variable gain amplifier (VGA) (Supplementary Fig. 1a). The front-end LNA is the most critical building block in setting the sensitivity of the overall amplifier, while the VGA provides an additional gain with tunability. The LNA is an operational amplifier (op-amp) placed in a closed negative feedback loop with capacitors C_1 and C_2 and pseudo-resistor R_{pseudo}. As the capacitor C_1 at the LNA input blocks DC currents to and from the nanoelectrodes, during the recording mode with the amplifier on, the nanoelectrodes work in the double-layer capacitive mode. The closed-loop topology of the LNA creates gain with bandpass characteristics, rejecting slow drift of the nanoelectrode voltage as well as the noise outside the signal frequency range. Its passband gain—from the LNA input V_{ne} to its output—is C_1/C_2. Since the VGA adopts the same topology as the LNA, its passband gain is C_1'/C_2', with these capacitors in reference to Supplementary Fig. 1a. This VGA

gain can be varied with the use of a tunable C_1', which is digitally controlled by the pixel memory (4 bits, Gain [1:4]). The passband gain of the overall amplifier is thus $G \equiv V_{amp}/V_{ne} = C_1/C_2 \times C_1'/C_2'$. The LNA input voltage, V_{ne}, is related to the electrical signal in solution, V_{sol} (Supplementary Fig. 8), via capacitive voltage division, $V_{ne}/V_{sol} = C_a/(C_a+C_p+C_1)$, where C_a is the double layer capacitance of the nanoelectrodes and C_p is the shunt stray capacitance of the V_{ne} node. The overall passband gain of the nanoelectrode-amplifier chain is then given by $V_{amp}/V_{sol} = C_1/C_2 \times C_1'/C_2' \times C_a/(C_a+C_p+C_1)$. This is the linear, flatband gain discussed in the main text; the cell-electrode interface is described in more detail in the following Supplementary Discussion "Modeling and measurement of nanoelectrode-cell interface."

The signal going through the nanoelectrode and amplifier is contaminated by noise. First, as the Johnson noise V_n from the nanoelectrode resistor R_a ($\overline{V}_n^2/\Delta f = 4kTR_a$; k: Boltzmann constant; T: temperature) stores a mean thermal energy of $kT/2$ onto the total capacitance $C_a+C_p+C_1$ at the amplifier's input node, the *rms* voltage noise at the amplifier input is $[kT/(C_a+C_p+C_1)]^{1/2}$ (this is a conservative calculation; actual noise is smaller due to the finite amplifier bandwidth). The amplifier adds noise, too, consisting of $1/f$ noise and thermal noise. Reducing this amplifier noise requires transistors in the signal path to be larger and sink more current, entailing trade-offs with the area and power. The pixel power, 12 μW, is designed to have limited adverse impact on room temperature *in vitro* cultures on top of the device. In sum, the design of the amplifier is a complex process to balance various parameters to optimize gain, noise, and ultimately the signal-to-noise ratio.

Setting the proper low and high cutoff frequencies of the amplifier bandpass characteristics is a critical task, to reject noise outside the bandwidth of electrophysiological signals. We aim at low cutoff frequency, f_1, of ~1 Hz, and high cutoff frequency, f_2, of ~5 KHz, to cover most

spectral contents of electrophysiological signals. The gain-bandwidth product is used to set $f_2 \sim 5$ kHz. To attain $f_1 \sim 1/(2\pi R_{pseudo} C_2) \sim 1$ Hz, R_{pseudo} should be on the order of TΩ, as C_2 is set at ~10 fF to optimize gain. Standard resistive materials in CMOS technology would occupy a prohibitively large area to produce such a large resistance: so we use anti-parallel *pn*-junction diode pairs biased at zero DC current as R_{pseudo} instead (Supplementary Fig. 1)—hence the name, pseudo-resistor. Here the anti-parallel connection makes the diode response symmetric for positive and negative signals. Moreover, to reduce nonlinearity of the resistor, we connect multiple pairs of anti-parallel diodes in series; this reduces voltage drop on each pair for a given signal, lessening nonlinearity.

In fact, we implement two types of pseudo-resistors to investigate trade-offs among various traits they impart on the amplifier. The pseudo-resistors in the LNAs in the top half of the array are 10 pairs of small anti-parallel diodes in series, while those in the LNAs in the bottom half are 3 pairs of large anti-parallel diodes. The former attains higher linearity, larger R_{pseudo}, and smaller parasitic capacitance. The VGA pseudo-resistors are 10 pairs of small anti-parallel diodes all across the array, as the linearity is of greatest importance in this second stage. The smaller parasitic capacitance of the top half anti-parallel diodes compared to bottom half anti-parallel diodes results in a larger gain, as seen in Fig. 2b. Other than the difference of gain, there is a slight difference in the input referred noise observed between these two designs (Supplementary Fig. 6).

The stimulator (buffer) to excite cells can apply a voltage signal with an amplitude of up to 4 V to the nanoelectrodes. At each pixel, the stimulator is accompanied by a 3-bit multiplexer (Stim[1:3]; Fig. 2, left); the latter chooses any one excitation signal from 3 different options that

are routed to all pixels and feeds the former. These variable options for stimulation are intended to make network studies more versatile.

The CMOS IC also includes, outside the pixel array, a digital block called 'memory write' (Supplementary Fig. 1). It receives configuration data bits (Config[1:10]) from a data acquisition (DAQ) card. It then programs the 1024 pixel memories sequentially; the programming of the entire array takes ~ 4.1 ms.

The 1024 amplifier outputs are divided into 8 subgroups, with each containing 128 outputs from 4 rows of the array. The 128 outputs in each subgroup feed a 128:1 analog output multiplexer of its own (Supplementary Fig. 1). This multiplexer continuously repeats, sampling the 128 outputs sequentially with a 1.248 MHz clock ('sample clock'; Supplementary Fig. 1). Each amplifier output is then sampled at an effective rate of 9.75 kHz with no aliasing up to 4.875 kHz—chosen close to f_2, the high cutoff of the amplifier. The 128 signals so sampled share the same data line. As a whole, 8 analog output data stream from the array, which are routed to 8 analog-to-digital converters of the DAQ card. For this multiplexing operation, the DAQ card produces the 1.248 MHz sample clock, which is fanned out to the 8 analog output multiplexers by an integrated digital block.

The biasing of the IC is facilitated by digitally programmable low-noise voltage regulators on the printed circuit board where the CMOS IC is mounted. They provide the IC with a power supply, 5 V, and amplifier input biases (V_{bias} in Supplementary Fig. 1), with reference to chip ground. The chip ground is programmable from -5.0 V to +5.0 V with 1-mV accuracy with respect to the potential V_{ref} of the Ag/AgCl reference electrode in solution, which we set at earth ground; the amplifier input biases are programmable with 0.5 mV accuracy. This biasing scheme allows pixel stimulators to produce both positive and negative voltages with respect to V_{ref}.

In addition to the voltage regulators, the printed circuit board contains an inline current sensing circuit to measure the positive and negative current through the reference electrode from ~1 pA to 1 μA.

Supplementary Discussion 2. Modeling and measurement of the nanoelectrode-cell interface

The models established in previous works[1–3] have been adopted here to represent the nanoelectrode-cell interface (Supplementary Fig. 8). In this model, the cell's membrane resistance and capacitance are designated as R_m and C_m, respectively, where the patch clamp electrode is assumed to have an ideal interface to manipulate and record the cell's membrane potential, V_m, and measure the corresponding current. After electroporation is performed using the nanoelectrodes, intracellular electrical access is achieved through the porous junctional membrane resistance, R_{jm}. The signal is attenuated, however, due to a seal resistance, R_s, between the nanoelectrode and cell membrane. This attenuated intracellular signal is recorded through the nanoelectrodes' access capacitance, C_a, biased in the capacitive region. Along the signal path to the pixel amplifier, current is shunted to the solution via the passivated metal pad's parasitic capacitance, C_p, and to ground through the input capacitance of the amplifier, C_1, causing a further attenuation. To record the signal, the nanoelectrode node, V_{ne}, is amplified, V_{amp}, and buffered off chip.

To extract the various circuit parameters, the nanoelectrodes are first characterized in extracellular solution (Supplementary Fig. 5). Cyclic voltammetry measurements show a wide capacitive region before faradaic current is passed, as expected for a Pt electrode. The access capacitance and parasitic capacitance are measured by applying a variable frequency sine wave, centered in the middle of the capacitive region, using the pixel stimulator to both a passivated control pad without nanoelectrodes (0 nanoelectrodes) and a normal pad with nanoelectrodes (9 nanoelectrodes). The current through the reference electrode is used to calculate the magnitude and phase of the impedances; the imaginary part of the impedance is used to calculate the

capacitance. The measurements show the highly capacitive nature of the nanoelectrodes with a calculated access capacitance of 1.2 pF and parasitic pad capacitance of 1.5 pF. These values are consistent with our theoretical calculation of the nanoelectrodes capacitance based on its material and geometries (a Pt cylinder 1μm tall and 150 nm in diameter with a unit double layer capacitance of 0.604 F/m^2).

Patch clamp experiments are then performed with HEK cells to measure the sum of the junctional membrane resistance and seal resistance, $R_{jm} + R_s$. The effective membrane resistance, R_{eff}, is determined by applying a 10 mV voltage pulse to the membrane using the patch clamp electrode, ΔV_m, and measuring the change of current, ΔI_m. As seen in Supplementary Fig. 8, R_{eff} changes from R_m to R_m in parallel with $R_{jm} + R_s$ after the nanoelectrodes' intracellular access is gained, shown in (1) and (2). From the experiments we calculate $R_{jm} + R_s$ to be in the range of 100 MΩ ~ 600 MΩ.

$$\text{Before access,} \quad R_{eff} = \frac{\Delta V_m}{\Delta I_m} = R_m \qquad (1)$$

$$\text{After access,} \quad R_{eff} = \frac{\Delta V_m}{\Delta I_m} = R_m \parallel \left(R_{jm} + R_s\right) \qquad (2)$$

Lastly, a range of values for R_{jm} and R_s are calculated from the attenuation ratio between V_m to V_{ne}. As R_s is significantly smaller than the impedance of C_a and C_p in the interested frequency range (~1 Hz - 5 kHz), the attenuation from V_m to V_{ne} is approximately multiplication of the resistive voltage divider between R_{jm} and R_s multiplied and the capacitive voltage divider between C_a and $C_p + C_1$, shown in (3). Throughout our HEK cell and cardiomyocyte experiments, we record attenuation factors ranging from 0.05 ~ 0.25, assuming an intracellular action potential amplitude of 120 mV for the cardiomyocytes. Together with the previous

measurements of C_a, C_p and $R_{jm} + R_s$, we calculate our R_s and R_{jm} to be in the range of 15 MΩ ~ 375 MΩ and 40 MΩ ~ 525 MΩ respectively.

$$\frac{V_{ne}}{V_m} \approx \frac{R_s}{R_s + R_{jm}} \times \frac{C_a}{C_a + C_p + C_1} \quad (3)$$

Supplementary Methods 1. CNEA fabrication and packaging

The CMOS IC that we designed was fabricated by Taiwan Semiconductor Manufacturing Company (Hsinchu, Taiwan) using the 2P4M, 3.3/5.0 V, 0.35 µm technology. The nanoelectrodes and packaging of the CNEA were post-fabricated in house; see Supplementary Figs. 2 and 3.

Supplementary Methods 2. Electrical characterization of CNEA

To measure the overall amplifier transfer function from V_{ne} to V_{amp} for a given pixel (Fig. 2b) as well as passband gain across the array (Fig. 2c), we applied a sine wave (0.5 mV amplitude and variable frequency ranging from 0.03 Hz to 50 kHz for Fig. 2b; 0.5 mV amplitude and 100 Hz for Fig. 2c) to each amplifier using the pixel stimulators. The results in Fig. 2c were sampled at 9.75 kHz, and a variable sample rate (>10× the applied sine wave) was used for Fig. 2b: a given amplifier can be sampled higher than the array sampling frequency of 9.75 kHz by stopping the analog multiplexer at an individual pixel, allowing measurement up to ~500 kHz. The output and input noise measurements of Supplementary Fig. 6 were performed by biasing the amplifier input using the stimulator; the input referred noise was calculated as the integrated output referred noise divided by the passband gain.

To characterize the nanowires-to-solution interface at an individual site, we apply a triangular voltage waveform (Supplementary Fig. 5, inset) to the nanowires using the stimulator at the site and measure the response current that flows between the nanowires and the Ag/AgCl reference electrode. The 2.5-V voltage range of the triangular waveform is centered near the zero current point: for the Pt nanowires, the center voltage is ~0.3 V vs. Ag/AgCl. The scan speed for the triangular waveform is 50 mV/s. For this experiment we use extracellular solution (136 mM

NaCl, 2.5 mM KCl, 10 mM HEPES, 10 mM D-glucose, 30 mM sucrose, 2 mM $CaCl_2$, 1.3 mM $MgCl_2$). For the electrical impedance spectroscopy we apply a 100 mV amplitude sine wave centered in the capacitive region and measure the resultant current through the reference electrode. To generate the nanoelectrode conductance map (Fig. 2d), we applied a 1.5 V DC stimulus *vs*. Ag/AgCl reference electrode in the extracellular solution and measured the resulting current between the nano- and reference electrodes after 100 ms. Pixels with conductive nanoelectrodes pass a Faradic current that is proportional to the metal surface area on the exposed tip. We designated pixels with currents measuring <30 pA as non-conductive and thus non-operative.

Supplementary Methods 3. Cardiomyocyte cell culture

We obtained cryopreserved neonatal rat ventricular myocytes from the ventricles of Sprague Dawley rats from QBM Cell Science (Ottawa, Canada) and plated them immediately upon arrival. The culture media contained 200 mL of RCBM base media and 0.2 mL GA-1000 (Lonza, Basel, Switzerland) with 15 mL of FBS and 15 mL of Horse serum (GE health care, Marlborough, MA). Before culture, the CNEA devices were first plasma treated (18 W, 10 min) and sterilized with 70% ethanol, coated with 100 µL of 50 µg /mL fibronectin (Sigma Aldrich, St Louis, MO), and incubated at 37°C for 1 hour. The cryopreserved cells were thawed in a 37°C water bath for 2 minutes, diluted with media and plated onto the device at a density of 300 K/mm^2. 80% of the media was exchanged 4 hours after plating and 50% was exchanged every two days afterwards.

Supplementary Methods 4. Cardiomyocyte electrophysiology and drug experiments

Neonatal rat ventricular cardiomyocytes were used for experiments 5 to 14 days after plating. The electrophysiology measurements were done in cell culture media at 37°C with an Ag/AgCl electrode as reference. During each experiment, simultaneous recording from 1024 pixels was performed for 3 to a maximum of 10 minutes, limited by a manageable file size of ~12 GB. To achieve the 20-minute extended measurement in Fig. 3c, we performed two consecutive 10-minute recordings and combined the data.

All pharmaceutical materials were purchased (Sigma Aldrich, St Louis, MO), prepared, and stored according to company recommendations. During the extracellular recording experiments (norepinephrine and 1-heptanol), the culture was perfused with media containing the reported concentration of drugs and incubated for 15 minutes before measurements. For the experiment with ATX-II, the toxin was applied 40 s after electroporation via perfusion. After measurement, media containing Ranolazine was then perfused and kept in the culture overnight until the next day's experiment.

Supplementary Methods 5. Electrical signal averaging and filtering

Intracellular recording data were filtered in the frequency domain by zeroing the fast Fourier transform (FFT) frequency content outside of the 1 Hz to 500 Hz frequency band and taking an inverse FFT. For comparison of intracellular action potential waveforms in Figs. 4c and 4d, we took averages of action potentials within a 5-10 s window. The individual action potentials were normalized to the maximum of the peak, aligned based on half of their peak height, and then averaged. Extracellular signals were digitally filtered in the time domain using a 300 Hz, single-pole high-pass filter.

Extracellular action potential peak times are extracted via time aligned averaging for better signal to noise ratio: ~400 ms windows around the spike time points (~200) from one pixel's recording were extracted and then used to align and average other pixel's recordings. The relative times of the resultant spikes in the averaged windows were then used as the peak time and for fittings of CVs and generating propagation maps (Figs. 3a & 4g). Pixels without spikes after averaging were discarded. For intracellular mappings (Figs. 3a & 4g) and videos (Supplementary Videos 2 & 3), the maximum peak times were extracted from pixel recordings that show clear intracellular signals.

Supplementary Methods 6. HEK cell culture and electrophysiology

Commercially available Human Embryonic Kidney (HEK) 293 cells (ATCC, Manassas, VA) were maintained according to company recommendations. During the experiment, the CNEA devices were first plasma treated and sterilized using 70% ethanol. The HEK293 cells were then passaged, plated onto the device, and incubated for at least 4 hours before experimentation. For whole-cell patch clamp, the culture media was changed into an extracellular solution (136 mM NaCl, 2.5 mM KCl, 10 mM HEPES, 10 mM D-glucose, 30 mM sucrose, 2 mM $CaCl_2$, 1.3 mM $MgCl_2$). Glass pipettes were filled with intracellular solution (120 mM K^+ gluconate, 10 mM Na^+ gluconate, 10 mM HEPES, 10 mM Na^+ phosphocreatine, 4 mM NaCl, 4 mM Mg-ATP, 2 mM Na_2-ATP, 0.3 mM Na_3-GTP) with a final impedance of 3 ~ 5 MΩ. Concurrent patch-clamp and nanoelectrode measurements were performed to the same cell to confirm the linear transfer function and the stimulation capability of the CNEA device. See Supplementary Fig. 7 caption for detailed results.

Supplementary Methods 7. Optical and fluorescence imaging

For fluorescent imaging of cardiomyocytes (Fig. 1e), the cells were incubated with 2 μM Calcein AM (Molecular Probes, Eugene, OR) for 15 minutes and imaged with a confocal microscope (Olympus Fluoview FV1000) using a 488 nm laser and 505-545 nm bandpass filter. The fluorescent images were taken in an array fashion and stitched together. Bright field microscope images and videos were taken using a differential interference contract (DIC) microscope (Olympus BX61W1). Cell movement in Fig. 2e was calculated as the sum of the absolute value of the frame-to-frame difference in the highlighted region of the picture of Fig. 2e, left.

Supplementary References

1. Robinson, J. T. *et al.* Vertical nanowire electrode arrays as a scalable platform for intracellular interfacing to neuronal circuits. *Nature Nanotech.* **7,** 180–184 (2012).
2. Spira, M. E. & Hai, A. Multi-electrode array technologies for neuroscience and cardiology. *Nature Nanotech.* **8,** 83–94 (2013).
3. Lin, Z. C., Xie, C., Osakada, Y., Cui, Y. & Cui, B. Iridium oxide nanotube electrodes for sensitive and prolonged intracellular measurement of action potentials. *Nat. Commun.* **5,** (2014).

Supplementary Video Captions

Supplementary Video 1 | Stimulation of a neonatal rat ventricular cardiomyocyte using a CNEA pixel. A cardiomyocyte sitting on top of a CNEA pixel (bottom) is induced to fire action potentials by applying a 1 V amplitude biphasic voltage pulse (top) every 1 s to the nanoelectrodes using the pixel stimulator. The centered vertical line represents real time in the video.

Supplementary Video 2 | Intracellular mapping of action potential propagation within a neonatal rat ventricular cardiomyocyte network using the CNEA. Intracellular action potentials are mapped across the CNEA device using peak times for the duration of 20-60 s after electroporation. The initial spiral pattern around the peripheral gives way to homogenous propagation due to membrane resealing around the nanoelectrodes.

Supplementary Video 3 | Induced spiral reentrant propagation in neonatal rat ventricular cardiomyocyte sheet. To promote reentrant propagation, the nanoelectrode array is reduced in size by covering ~6 peripheral rows of pixels with PDMS and rounded. The center region is then electroporated to cause leakage currents, promoting a reduced conduction velocity and allowing for a concave propagation wavefront.

Supplementary Video 4 | Intracellular mapping of action potential and ATX-II induced early afterdepolarizations (EADs) within a neonatal rat ventricular cardiomyocyte network using the CNEA. The analog voltages recorded by each pixel amplifier are normalized and translated into gray scale for visualization for the duration of 239-242 s after electroporation (corresponding to the traces in Fig. 4f). The video is reduced to 1/5 play speed. Local propagation dynamics are seen on the left half of the cardiomyocyte sheet where triggered activity and EADs are observed.