

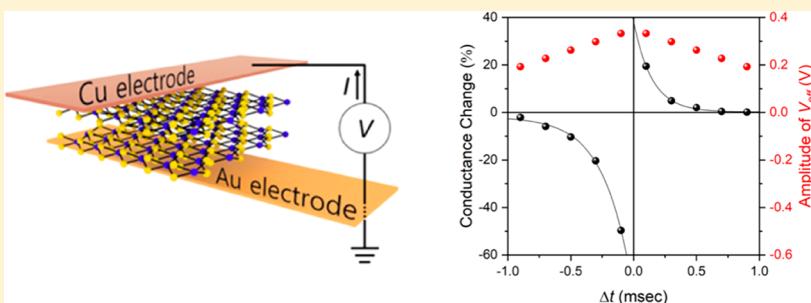
Vertical MoS₂ Double-Layer Memristor with Electrochemical Metallization as an Atomic-Scale Synapse with Switching Thresholds Approaching 100 mV

Renjing Xu,^{†,§} Houk Jang,^{†,§} Min-Hyun Lee,[‡] Dovran Amanov,[†] Yeonchoo Cho,[‡] Haeryong Kim,[‡] Seongjun Park,[‡] Hyeyoung Shin,^{*,‡,ID} and Donhee Ham^{*,†,ID}

[†]School of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts 02138, United States

[‡]Samsung Advanced Institute of Technology, Samsung Electronics, Suwon 443-803, South Korea

Supporting Information



ABSTRACT: Atomically thin two-dimensional (2D) materials—such as transition metal dichalcogenide (TMD) monolayers and hexagonal boron nitride (hBN)—and their van der Waals layered preparations have been actively researched to build electronic devices such as field-effect transistors, junction diodes, tunneling devices, and, more recently, memristors. Two-dimensional material memristors built in lateral form, with horizontal placement of electrodes and the 2D material layers, have provided an intriguing window into the motions of ions along the atomically thin layers. On the other hand, 2D material memristors built in vertical form with top and bottom electrodes sandwiching 2D material layers may provide opportunities to explore the extreme of the memristive performance with the atomic-scale interelectrode distance. In particular, they may help push the switching voltages to a lower limit, which is an important pursuit in memristor research in general, given their roles in neuromorphic computing. In fact, recently Akinwande et al. performed a pioneering work to demonstrate a vertical memristor that sandwiches a single MoS₂ monolayer between two inert Au electrodes, but it could neither attain switching voltages below 1 V nor control the switching polarity, obtaining both unipolar and bipolar switching devices. Here, we report a vertical memristor that sandwiches two MoS₂ monolayers between an active Cu top electrode and an inert Au bottom electrode. Cu ions diffuse through the MoS₂ double layers to form atomic-scale filaments. The atomic-scale thickness, combined with the electrochemical metallization, lowers switching voltages down to 0.1–0.2 V, on par with the state of the art. Furthermore, our memristor achieves consistent bipolar and analogue switching, and thus exhibits the synapse-like learning behavior such as the spike-timing dependent plasticity (STDP), the very first STDP demonstration among all 2D-material-based vertical memristors. The demonstrated STDP with low switching voltages is promising not only for low-power neuromorphic computing, but also from the point of view that the voltage range approaches the biological action potentials, opening up a possibility for direct interfacing with mammalian neuronal networks.

KEYWORDS: Memristor, resistive memory, analogue neural network, neuromorphic computing, two-dimensional materials, transition metal dichalcogenide, spike-timing dependent plasticity

Two-dimensional (2D) crystals—such as transition metal dichalcogenide (TMD) monolayers and hexagonal boron nitride (hBN)—and their van der Waals layered preparations have been an active pursuit of basic and applied research. With electronics being one of their key target application areas, the 2D materials have been used to build a variety of electronic devices such as field-effect transistors (FETs),^{1,2} junction diodes,^{3,4} tunneling devices,^{5,6} and, relatively more recently, memristors,^{7–19} two-terminal nonvolatile resistive memory. These

memristors have harnessed the unique 2D material properties to hit a number of intriguing performance milestones, e.g., fJ dissipation per resistive switching with sub-pA current;⁸ 8 GHz operation;⁷ or operation up to 340 °C.⁹ At the system level, the 2D material memristors as memory elements may be integrated

Received: December 25, 2018

Revised: March 12, 2019

Published: March 21, 2019

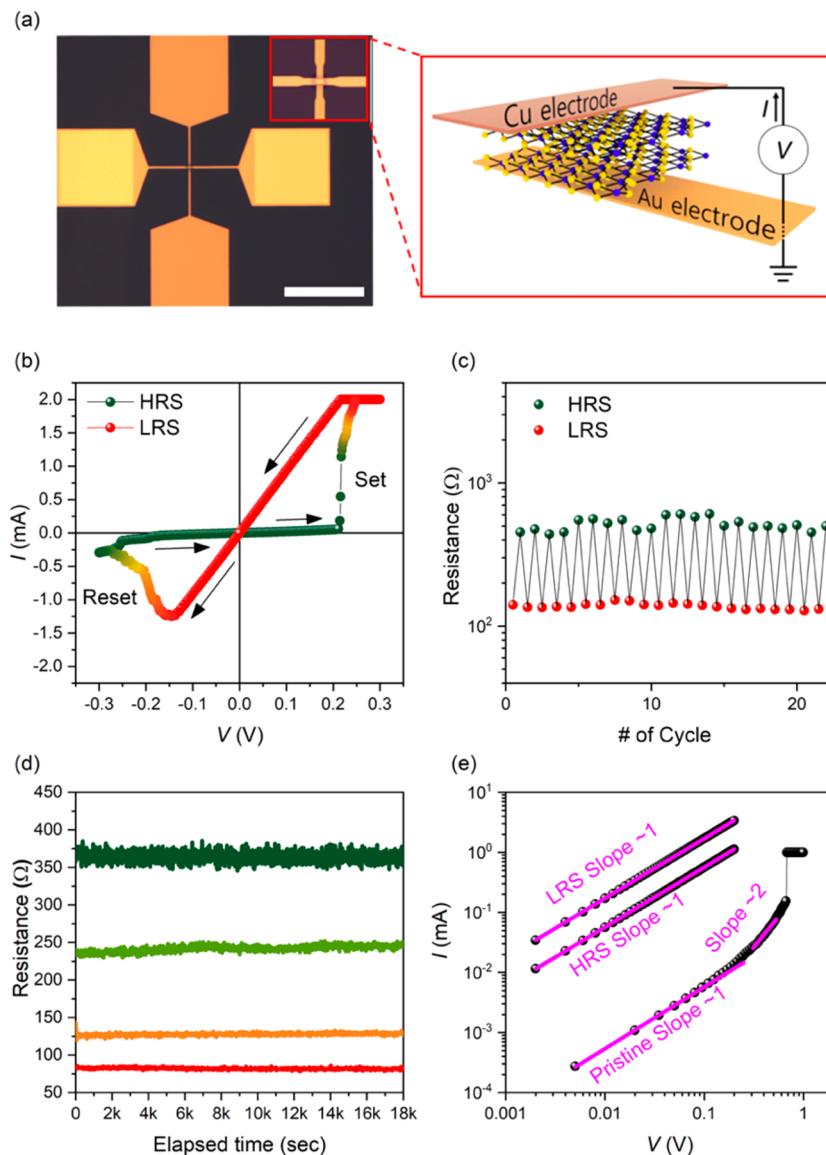


Figure 1. Cu/MoS₂ double-layer/Au memristor. (a) Optical image with the scale bar of 100 μm (left) and schematic illustration (right). In the optical image, two probe pads (orange) connect to the bottom Au electrode, while the other two probe pads (yellow) connect to the top Cu electrode. The memristor's crossbar area is $2 \times 2 \mu\text{m}^2$. (b) Measured I - V curve (DC sweep) of the memristor clearly shows the bipolar resistive switching with a set voltage at ~ 0.25 V and a reset voltage at ~ -0.15 V. (c) Resistances of HRS and LRS through multiple DC I - V sweeps. (d) Measured retention of various resistive states at room temperature (read voltage: 10 mV). (e) Logarithm scale I - V curves (black spheres) and fitted curves (solid pink lines) for the pristine state before the forming occurs, and for the LRS and HRS states after the forming.

with 2D material FETs to perform complex electronic functions. In particular, they can be used as artificial synapses to build analogue neural networks and neuromorphic circuits in the 2D material platform.

Two-dimensional material memristors have been implemented in both lateral and vertical forms. In the lateral form, TMD layers—such as MoS₂ layers—are arranged horizontally with two terminal electrodes.^{10–12} These lateral structures have opened up an intriguing window to study the motions of ions such as sulfur vacancies *along* the TMD layers as a mechanism underlying the memristive effect. However, the distance between the two lateral electrodes flanking the TMD layers has thus far been on the order of micrometers, resulting in relatively large switching voltages (20–100 V). In contrast, the vertical structures^{8,13–18} sandwich 2D material layers—such as MoS₂, MoS₂/MoO_x, and hBN—between top and bottom

electrodes, substantially reducing the interelectrode distance just *across* the 2D material layers. This vertical distance in the range of tens of nanometers^{16–18,20–22} has achieved substantially lower switching voltages (1–10 V), and the vertical distance down to a few nanometers^{8,13–15} has further driven down the switching voltages below 1 V.

It would be valuable, therefore, to go to the extreme and to build a vertical memristor with one or two TMD monolayers to study whether such atomically thin layers could still serve as a memristive medium and, if so, what the limit of the memristive performance would be. In particular, such atomic-scale interelectrode distance may help push the switching voltages to a lower limit, which is one of the critical pursuits in the research of memristors in general, given their roles as artificial synapses in neuromorphic computing. In fact, the work in refs 7 and 19 pioneered such a vertical structure with a single MoS₂

monolayer sandwiched between two Au electrodes, where a memristive behavior was indeed observed. However, this work reported both bipolar and unipolar devices without being able to control the resistive switching polarity. Also, the switching voltage was not below 1 V—which is even larger than the vertical memristors employing several 2D layers^{8,13–15}—indicating that factors other than atomic thickness may be affecting the switching voltages in this particular implementation.

Here, we further explore vertical 2D material memristors with atomic-scale thickness, reporting a MoS₂ double-layer memristor sandwiched by a top Cu electrode and a bottom Au electrode (Figure 1a). Our Cu/MoS₂ double-layer/Au structure differs from the Au/MoS₂ monolayer/Au structure of refs 7 and 19 in two ways. First, we use two MoS₂ monolayers (in our particular implementation, a single MoS₂ monolayer does not produce a reliable memristive effect, as discussed later). Second, we use active Cu as the top electrode while the bottom electrode is still inert Au. Cu ions diffuse through the MoS₂ double layers to form atomic-scale filaments. Our memristor is thus an electrochemical metallization memory (ECM) device, whereas the memristor of refs 7 and 19 is likely to be a valence change memory (VCM) device where sulfur vacancies move to form conductive channels. Our structure achieves switching voltages of 0.1–0.2 V, which is substantially lower than ~1 V of refs 7 and 19; this is because Cu has a lower migration barrier and diffusion activation energy in MoS₂ than sulfur vacancies.^{23–25} Such low switching voltages of our structure—enabled by the combination of the atomic-scale thickness and electrochemical metallization—are important, especially for neuromorphic computing, which strives to operate with a power far lower than digital computing. Furthermore, our asymmetric structure consistently exhibits bipolar switching (16 out of 16 tested devices), and it also assumes more than two resistive states. The combination of these two traits—bipolar and analog—leads to the synapse-like learning behavior, such as the spike-timing dependent plasticity (STDP): this is the first demonstration of STDP among all vertical memristor work involving 2D materials. Not only is the STDP with low switching voltages important for neuromorphic computing, but it also can open up new directions of directly interfacing with the mammalian neuronal networks, as the switching voltages approach the action potentials of biological neurons.

The bottom electrode (35 nm Au and 5 nm Cr) is patterned on SiO₂/Si substrate via standard photolithography. Large-area MoS₂ monolayers synthesized by metal–organic chemical vapor deposition (MOCVD; see Figure S1 for the Raman and photoluminescence characterizations) are then transferred layer by layer through a vacuum stack process onto the bottom Au electrode to form a precisely double-layer stack.²⁶ The top electrode (35 nm Cu) is then defined on top of the double-layer MoS₂. The crossbar area of the memristor is $2 \times 2 \mu\text{m}^2$ (Figure 1a).

This MoS₂ double layer between the Cu and Au electrodes unequivocally exhibits bipolar resistive switching and non-volatility (Figure 1b–d). The DC current–voltage (I – V) curve (Figure 1b), obtained with the voltage sweep range from −0.3 to 0.3 V and a sweep rate of 0.15 V/s (sweep step, 3 mV; duration for each step, 20 ms), shows bipolar resistive switching with the set and reset voltages of ~0.25 and ~−0.15 V. As mentioned earlier, these low switching voltages are attributed to the atomic-scale thickness of the memristive media and the low energy barrier for Cu ions to diffuse through the MoS₂ double layer.²³ When we repeated the I – V sweep several times within the same

voltage polarity, we could not set and reset the device (Figure S2; see also Figure 3b), which confirms that our device is a bipolar resistive switch. The I – V curve in Figure 1b (and also see Figures 2c and 3b) also shows that the device, on either voltage polarity, can assume a range of resistance values between the high resistance state (HRS) and the low resistance state (LRS) values, demonstrating that the device is not only bipolar but also analogue. This point will be discussed further later. Over 20 cycles of the I – V sweeps, the device rather stably maintained the HRS and LRS resistance values (Figure 1c). The device could retain a given resistance state at least for ~5 h at room temperature (Figure 1d).

While the majority of these double-layer MoS₂ memristors are free of the forming process (Figure S3), we can use a double-layer MoS₂ memristor that exhibits the forming to provide further insight into the transport mechanism. The I – V curves of the example device measured for the pristine state (before the forming occurs) as well as for the HRS and LRS (after the forming) are juxtaposed in Figure 1e in the logarithmic scale. In the pristine state, the I – V curve shows a slope of ~1 for the voltage up to 0.3 V with an extracted resistance of ~16.6 kΩ. The conduction mechanism here is quantum tunneling,^{27–30} and this resistance in the pristine state is much larger than the range of resistances obtained later after the forming. As the voltage increases beyond 0.3 V in the pristine state, the logarithmic-scale I – V curve transitions into a slope 2 region ($I \propto V^2$) for the voltage up to 0.6 V, which corresponds to a space-charge-limited conduction.^{27,28} As the voltage is further increased, the current dramatically increases, corresponding to the forming of Cu filaments: that is, with the high enough positive voltage, the top Cu electrode is oxidized, and the resulting Cu ions migrate to the bottom Au electrode, where Cu ions are reduced and deposited.^{29,31} Thus, the Cu filaments build up to bridge the Au and Cu electrodes. These Cu filaments are likely to form preferentially along the defective grain boundaries^{32,33} [see Figure S4 for the image of example grain boundaries in an MOCVD-grown MoS₂ monolayer, obtained by a scanning transmission electron microscope (STEM) with high-angle annular dark-field imaging (HAADF)]. This is supported by our simulation based on the first-principle density functional theory, which shows that the diffusion through the crystalline part of the MoS₂ monolayer requires a much higher energy (~3.9 eV) than that through the grain boundaries (~0.3 eV) (Figure S5).

After the forming, the logarithmic-scale I – V curves for both the HRS and LRS clearly exhibit ohmic conduction slopes of ~1 with extracted resistances of ~180 and ~50 Ω, respectively. The ohmic conduction observed in the HRS suggests that the Cu filaments may still bridge the top and bottom electrodes even in the HRS, while the overall cross-sectional area of the filaments—which reflects both the number of filaments and the cross-sectional area of each individual filament—may be smaller in the HRS. The LRS to HRS transition (reset) requires switching the voltage from positive to negative polarity, which collects the Cu atoms in the filaments back to the top Cu electrode, hence reducing the overall cross-sectional area of the Cu filaments. This is consistent with the observed bipolar switching (such bipolar switching with Cu filaments is well-known³⁴ in oxide-based memristive media with switching voltages of ~1 V). In fact, all 16 test devices with the Cu/MoS₂ double-layer/Au structure consistently exhibited bipolar resistive switching.

As a control experiment to corroborate the forgoing resistive switching mechanism, we tested 8 devices with the structure of Au/MoS₂ double-layer/Au. First, all of them consistently

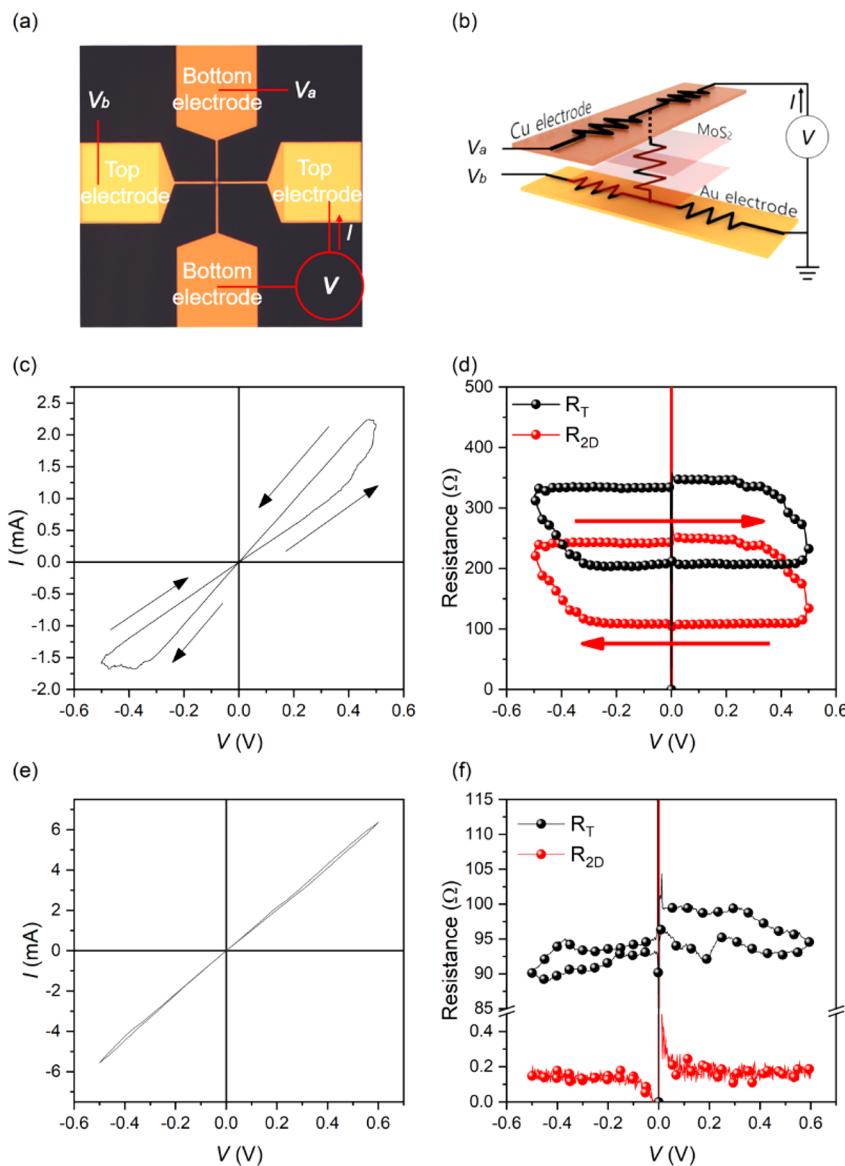


Figure 2. Four-point probe measurements. (a, b) Four-probe measurement setup to measure total resistance R_T and resistance R_{2D} across MoS₂. (c, d) Measured I – V curve of a Cu/MoS₂ double-layer/Au memristor and measured R_T and R_{2D} as functions of voltage. (e, f) Measured I – V curve of a Cu/MoS₂ monolayer/Au memristor and measured R_T and R_{2D} as functions of voltage.

exhibited unipolar switching with their symmetric structure. Second, the set and reset voltages for these unipolar devices are ~1.2 and 0.6–0.8 V, respectively (Figure S6), which are much larger than those of the bipolar devices (0.1–0.2 V). The unipolar devices are likely to be a VCM that forms the conductive channels based on sulfur vacancies: sulfur vacancies have much larger migration barrier and diffusion activation energy in MoS₂,^{24,25} as compared to those of Cu in MoS₂,²³ which explains the larger set and reset voltages of the unipolar devices.

Four-point probe measurements provide further information about the memristive behavior of our bipolar device (Cu/MoS₂ double-layer/Au). Four probes land on the four metallic pads as shown in Figure 2a, where two pads are connected to the top electrode, and the other two pads are connected to the bottom electrode. As illustrated in Figure 2a,b, two probes are used to apply voltage V across the memristive device and measure the resulting current I , whereas the other two probes are used to measure voltages V_a and V_b at the corresponding pad positions

as shown in the figures. Then the total resistance R_T between the top and bottom pads across which V is applied and the resistance R_{2D} directly across the MoS₂ double layer are given, respectively, by $R_T = V/I$ and $R_{2D} = (V_a - V_b)/I$. The results of this four-probe measurement for our Cu/MoS₂ double-layer/Au structure (Figure 2c,d)—whose essence is consistent across 8 four-probe tested devices (Figure S7)—reveal that R_{2D} exhibits a clear hysteresis, and R_T simply follows this hysteresis, confirming that the memristive behavior does originate from the MoS₂ double-layer region.

In contrast, as we perform the four-probe measurement for a vertical structure with Cu and Au electrodes but with a single MoS₂ monolayer (Figure 2e,f), no appreciable hysteresis is observed in R_{2D} , which is also substantially smaller, nearing zero. In fact, 12 such single MoS₂ monolayer devices tested with four-probe methods consistently exhibited no hysteresis in nearly zero R_{2D} (Figure S7). This indicates that a single MoS₂ monolayer does not give the memristive behavior, but it rather shorts the top and bottom electrodes with current passing

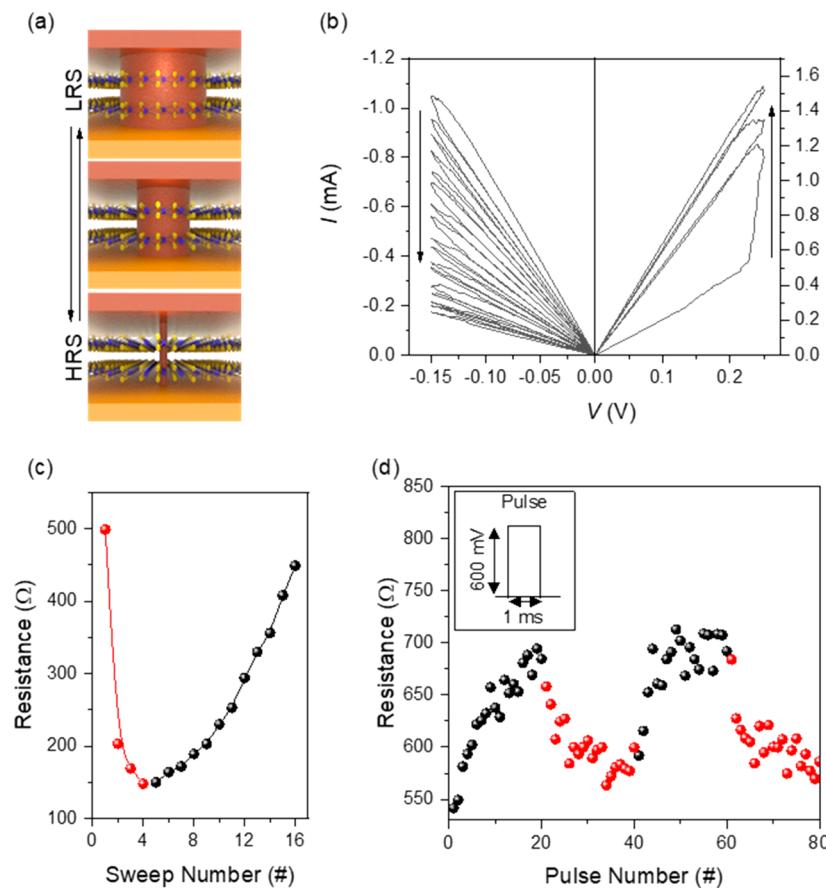


Figure 3. Bipolar, analogue switch as an artificial synapse. (a) The change of the resistance of the Cu/MoS₂ double-layer/Au memristor is likely to originate from the cumulative area change of the Cu filaments. (b) Consecutive positive voltage sweeps continue to increase the conductance (potentiation, right) whereas consecutive negative voltage sweeps continue to decrease the conductance (depression, left). (c) Memristor resistance value at 0.1 V after each voltage sweep, corresponding to part b. Here, the red dots are after the positive voltage sweeps, whereas the black dots are after the negative voltage sweeps. (d) Manipulation of the memristor resistance with positive and negative voltage pulses. In this measurement example, potentiation (red dot) is achieved with a positive pulse with an amplitude of 0.6 V and a duration of 1 ms, while depression (black dot) is achieved with a negative pulse with an amplitude of 0.6 V and a duration of 1 ms. The resistance after each pulse is measured with a small read voltage of 10 mV.

through the MoS₂ monolayer. Such pass through may result from defects and cracks introduced during transfer processes or metal deposition. On the other hand, the chance of the pass-through locations of each layer to overlap across two layers is small, hence making the memristive behavior possible with the MoS₂ double layer.

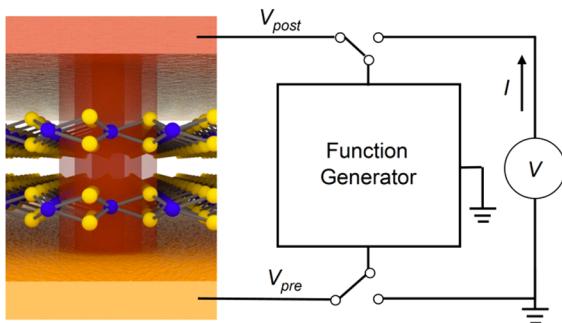
As another control, we also fabricate and measure 12 MoS₂ triple-layer devices with top Cu and bottom Au electrodes (Figure S3). These triple-layer devices exhibit clear memristive behaviors like the double-layer MoS₂ devices, with similar HRS/LRS resistances and on/off ratios. On the other hand, while 15 out of the 16 double-layer MoS₂ memristors are forming free, all of the 12 triple-layer MoS₂ memristors require the forming process, as bridging top and bottom electrodes with filaments becomes increasingly more difficult with the growing number of layers. Similarly, the switching thresholds (~ 0.36 V for set and ~ -0.28 V for reset) of the triple-layer devices are overall larger than those (~ 0.22 V for set and ~ -0.14 V for reset) of the double-layer devices.

As seen earlier, our device manifests not only bipolar but also analogue resistance switching, and thus, it can serve as an artificial synapse. We first measure the depression and potentiation with DC voltage sweeps. As we repeat several times a positive-polarity voltage sweep in the range 0–0.25 V, the device resistance gradually decreases from ~ 450 to ~ 150 Ω

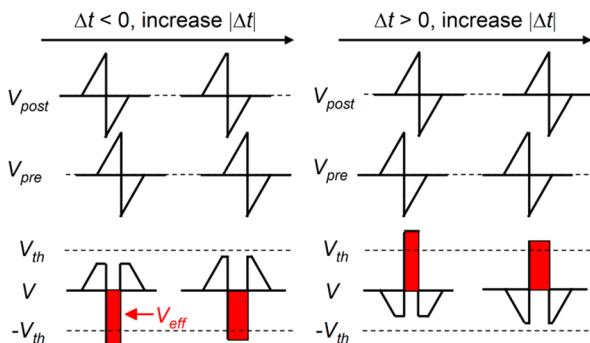
(potentiation), but as we subsequently repeat several times a negative-polarity voltage sweep in the range from 0 to -0.15 V, the device resistance gradually decreases back to ~ 500 from ~ 150 Ω (depression): see Figure 3b,c. This experiment clearly shows again the existence of many internal resistive states—i.e., analogue nature of the device—and bipolar switching (and the lack of unipolar behavior). For any given resistive state encountered in this experiment of Figure 3b, every logarithmic-scale I – V curve shows an ohmic conduction with a slope of 1. This reconfirms our earlier notion that the bottom and top electrodes may be always connected with the Cu filaments, with the resistance of a given state being set by the overall cross-sectional area of the Cu filaments³⁵ (this is conceptually illustrated in Figure 3a). We can cause the potentiation and depression in a pulsed mode experiment as well (Figure 3d). For example, we apply a sequence of 20 negative pulses (pulse amplitude of -0.6 V, pulse duration of 1 ms) and subsequently a sequence of 20 positive pulses (pulse amplitude of 0.6 V, pulse duration of 1 ms), where the pulse-to-pulse time interval is ~ 5 s. The device resistance is measured after each pulse with a small read voltage of 10 mV. As expected from the DC sweep experiment, the negative pulses gradually increase the device resistance (depression), and the positive pulses gradually decrease the device resistance (potentiation).

The foregoing experiment of Figure 3 demonstrates artificial synaptic plasticity, an important component for neuromorphic circuits.³⁶ We further study the synaptic plasticity in our device, this time, by demonstrating the STDP^{36–38} (Figure 4). To this

(a)



(b)



(c)

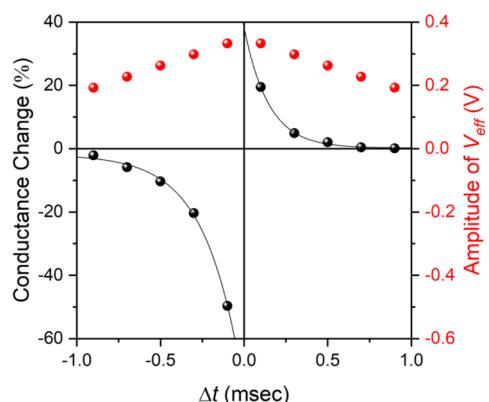


Figure 4. Demonstration of STDP. (a) Measurement setup. (b) Postsynaptic and presynaptic voltage pulses, V_{post} and V_{pre} , applied at the top and bottom electrodes, and $V = V_{\text{post}} - V_{\text{pre}}$ across the memristor, for different values of Δt , the arrival time difference for the post- and presynaptic pulses. (c) STDP: the measured change of the memristor conductance (synaptic weight) and the amplitude of the effective voltage as a function of Δt .

end, the top Cu and the bottom Au electrodes are driven, respectively, by two voltage signals, V_{post} and V_{pre} , which we call post- and presynaptic pulses (Figure 4a). We choose V_{post} and V_{pre} to have the same shape, linearly increasing from 0 to 0.175 V for a duration of 1 ms and then from -0.175 to 0 V for another duration of 1 ms,³⁹ but they arrive generally at two different times t_{pre} and t_{post} with the time difference being $\Delta t = t_{\text{post}} - t_{\text{pre}}$.

The voltage V across the memristor is $V = V_{\text{post}} - V_{\text{pre}}$. This V is illustrated in Figure 4b for various values of Δt , and is compared to the estimated switching voltages ± 0.175 V of the memristor under test, where we define $V_{\text{th}} = 0.175$ V. For $\Delta t < 0$, the positive part of V is always smaller than V_{th} while the negative part of V can exceed V_{th} in magnitude, so we ignore the former and consider only the latter, calling it V_{eff} (so $V_{\text{eff}} < 0$ for $\Delta t < 0$). Likewise, for $\Delta t > 0$, the negative part of V is always smaller than V_{th} in magnitude while the positive part of V can exceed V_{th} , so we consider only the latter as V_{eff} (so $V_{\text{eff}} > 0$ for $\Delta t > 0$). Figure 4b shows that the amplitude of V_{eff} increases with decreasing $|\Delta t|$.

Therefore, if the presynaptic pulse comes before the postsynaptic pulse ($\Delta t > 0$), the memristor is driven into the positive voltage polarity ($V_{\text{eff}} > 0$) and hence undergoes a potentiation. If the magnitude of this positive Δt is smaller, the driving into the positive voltage polarity is stronger (because the amplitude of V_{eff} is larger), and hence, the degree of potentiation becomes stronger. Similarly, if the postsynaptic pulse comes before the presynaptic pulse ($\Delta t < 0$), the memristor is driven into the negative voltage polarity ($V_{\text{eff}} < 0$) and hence undergoes a depression. If the magnitude of this negative Δt is smaller, the driving into the negative voltage polarity is stronger (because the amplitude of V_{eff} is larger), and hence, the degree of depression becomes stronger. In fact, these constitute STDP, which we have experimentally confirmed as shown in Figure 4c. Each black dot for a given $\Delta t > 0$ represents a conductance change from the HRS after driving the memristor once with a pair of the pre-/postsynaptic pulses with the given Δt . Each black dot for a given $\Delta t < 0$ is obtained similarly, but the conductance changes for each given Δt measured from the LRS. The change in the conductance versus Δt on either the positive or negative side can be fit with an exponential decay.³⁵

This demonstration of STDP combined with the low switching voltages of 0.1–0.2 V is promising for the application in neuromorphic circuits, as the synaptic learning rule and low-power computation are some of the key ingredients of neuromorphic engineering. While the device current is relatively high with the relatively low HRS and LRS resistances of the memristors presented thus far with the crossbar area of $2 \times 2 \mu\text{m}^2$, this is a matter of scaling: we can readily increase the resistance by lessening the crossbar area, thus by reducing the number of Cu filaments. In fact, our measurement of three additional MoS₂ double-layer memristors with decreased crossbar areas ($1 \times 1 \mu\text{m}^2$, $0.5 \times 0.5 \mu\text{m}^2$, $0.1 \times 0.1 \mu\text{m}^2$) indeed supports the scaling (Figure S8), increasing the HRS and LRS resistances up to ~ 4 G Ω and ~ 6 k Ω with the large HRS/LRS resistance ratio. Since our individual device work was done by layer-by-layer stacking of large-area MOCVD-grown MoS₂ monolayers, it can now be readily scaled into a circuit-level work to build memory arrays as part of analogue neural networks as well as neuromorphic circuits.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: [10.1021/acs.nanolett.8b05140](https://doi.org/10.1021/acs.nanolett.8b05140).

Photoluminescence and Raman spectra, bipolar resistive switching, comparison of Cu/MoS₂ double-layer/Au and Cu/MoS₂ triple-layer/Au devices, STEM image, simulation of Cu diffusion, unipolar resistive switching of Au/

MoS₂ double-layer/Au, four-point probe measurements, and scaling behavior ([PDF](#))

AUTHOR INFORMATION

Corresponding Authors

*E-mail: hyeonjin.shin@samsung.com.
*E-mail: donhee@seas.harvard.edu.

ORCID

Hyeon-jin Shin: [0000-0002-6992-6341](https://orcid.org/0000-0002-6992-6341)

Donhee Ham: [0000-0001-6925-2466](https://orcid.org/0000-0001-6925-2466)

Author Contributions

[§]R.X. and H.J. contributed equally to this work.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors acknowledge the support by Samsung Electronics on the collaborative research for two-dimensional materials and their applications, and the support by the National Science Foundation STC Center for Integrated Quantum Materials under Contract DMR-1231319. Device fabrication was performed in part at the Center for Nanoscale Systems at Harvard University.

REFERENCES

- (1) Xia, F.; Farmer, D. B.; Lin, Y. -m.; Avouris, P. *Nano Lett.* **2010**, *10* (2), 715–718.
- (2) Lee, G.-H.; Yu, Y.-J.; Cui, X.; Petrone, N.; Lee, C.-H.; Choi, M. S.; Lee, D.-Y.; Lee, C.; Yoo, W. J.; Watanabe, K.; Taniguchi, T.; Nuckolls, C.; Kim, P.; Hone, J. *ACS Nano* **2013**, *7* (9), 7931–7936.
- (3) Deng, Y.; Luo, Z.; Conrad, N. J.; Liu, H.; Gong, Y.; Najmaei, S.; Ajayan, P. M.; Lou, J.; Xu, X.; Ye, P. D. *ACS Nano* **2014**, *8* (8), 8292–8299.
- (4) Buscema, M.; Groenendijk, D. J.; Steele, G. A.; van der Zant, H. S. J.; Castellanos-Gomez, A. *Nat. Commun.* **2014**, *5*, 4651.
- (5) Lee, G.-H.; Yu, Y.-J.; Lee, C.; Dean, C.; Shepard, K. L.; Kim, P.; Hone, J. *Appl. Phys. Lett.* **2011**, *99* (24), 243114.
- (6) Britnell, L.; Gorbachev, R. V.; Jalil, R.; Belle, B. D.; Schedin, F.; Mishchenko, A.; Georgiou, T.; Katsnelson, M. I.; Eaves, L.; Morozov, S. V.; Peres, N. M. R.; Leist, J.; Geim, A. K.; Novoselov, K. S.; Ponomarenko, L. A. *Science* **2012**, *335* (6071), 947.
- (7) Kim, M.; Ge, R.; Wu, X.; Lan, X.; Tice, J.; Lee, J. C.; Akinwande, D. *Nat. Commun.* **2018**, *9* (1), 2524.
- (8) Zhao, H.; Dong, Z.; Tian, H.; DiMarzi, D.; Han, M. G.; Zhang, L.; Yan, X.; Liu, F.; Shen, L.; Han, S. J.; Cronin, S.; Wu, W.; Tice, J.; Guo, J.; Wang, H. *Adv. Mater.* **2017**, *29* (47), 1703232.
- (9) Wang, M.; Cai, S.; Pan, C.; Wang, C.; Lian, X.; Zhuo, Y.; Xu, K.; Cao, T.; Pan, X.; Wang, B.; Liang, S.-J.; Yang, J. J.; Wang, P.; Miao, F. *Nat. Electron.* **2018**, *1* (2), 130–136.
- (10) Sangwan, V. K.; Lee, H. S.; Bergeron, H.; Balla, I.; Beck, M. E.; Chen, K. S.; Hersam, M. C. *Nature* **2018**, *554* (7693), 500–504.
- (11) Sangwan, V. K.; Jariwala, D.; Kim, I. S.; Chen, K. S.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C. *Nat. Nanotechnol.* **2015**, *10* (5), 403–6.
- (12) Li, D.; Wu, B.; Zhu, X.; Wang, J.; Ryu, B.; Lu, W. D.; Lu, W.; Liang, X. *ACS Nano* **2018**, *12* (9), 9240–9252.
- (13) Bessonov, A. A.; Kirikova, M. N.; Petukhov, D. I.; Allen, M.; Ryhänen, T.; Bailey, M. J. A. *Nat. Mater.* **2015**, *14* (2), 199–204.
- (14) Pan, C.; Ji, Y.; Xiao, N.; Hui, F.; Tang, K.; Guo, Y.; Xie, X.; Puglisi, F. M.; Larcher, L.; Miranda, E.; Jiang, L.; Shi, Y.; Valov, I.; McIntyre, P. C.; Waser, R.; Lanza, M. *Adv. Funct. Mater.* **2017**, *27* (10), 1604811.
- (15) Qian, K.; Tay, R. Y.; Nguyen, V. C.; Wang, J.; Cai, G.; Chen, T.; Teo, E. H. T.; Lee, P. S. *Adv. Funct. Mater.* **2016**, *26* (13), 2176–2184.
- (16) Shin, G. H.; Kim, C.-K.; Bang, G. S.; Kim, J. Y.; Jang, B. C.; Koo, B. J.; Woo, M. H.; Choi, Y.-K.; Choi, S.-Y. *2D Mater.* **2016**, *3* (3), No. 034002.
- (17) Son, D.; Chae, S. I.; Kim, M.; Choi, M. K.; Yang, J.; Park, K.; Kale, V. S.; Koo, J. H.; Choi, C.; Lee, M.; Kim, J. H.; Hyeon, T.; Kim, D. H. *Adv. Mater.* **2016**, *28* (42), 9326–9332.
- (18) Tan, C.; Zhang, H. *Chem. Soc. Rev.* **2015**, *44* (9), 2713–31.
- (19) Ge, R.; Wu, X.; Kim, M.; Shi, J.; Sonde, S.; Tao, L.; Zhang, Y.; Lee, J. C.; Akinwande, D. *Nano Lett.* **2018**, *18* (1), 434–441.
- (20) Liu, J.; Zeng, Z.; Cao, X.; Lu, G.; Wang, L. H.; Fan, Q. L.; Huang, W.; Zhang, H. *Small* **2012**, *8* (22), 3517–22.
- (21) Hao, C.; Wen, F.; Xiang, J.; Yuan, S.; Yang, B.; Li, L.; Wang, W.; Zeng, Z.; Wang, L.; Liu, Z.; Tian, Y. *Adv. Funct. Mater.* **2016**, *26* (12), 2016–2024.
- (22) Lee, M. J.; Lee, S.; Lee, S.; Balamurugan, K.; Yoon, C.; Jang, J. T.; Kim, S.-H.; Kwon, D.-H.; Kim, M.; Ahn, J.-P.; Kim, D. H.; Park, J.-G.; Park, B. H. *NPG Asia Mater.* **2018**, *10* (4), 23–30.
- (23) Guzman, D. M.; Onofrio, N.; Strachan, A. *J. Appl. Phys.* **2017**, *121* (5), No. 055703.
- (24) Komsa, H.-P.; Kurasch, S.; Lehtinen, O.; Kaiser, U.; Krasheninnikov, A. V. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2013**, *88* (3), No. 035301.
- (25) Le, D.; Rawal, T. B.; Rahman, T. S. *J. Phys. Chem. C* **2014**, *118* (10), 5346–5351.
- (26) Kang, K.; Lee, K. H.; Han, Y.; Gao, H.; Xie, S.; Muller, D. A.; Park, J. *Nature* **2017**, *550* (7675), 229–233.
- (27) Wang, C.; He, W.; Tong, Y.; Zhao, R. *Sci. Rep.* **2016**, *6*, 22970.
- (28) Chiu, F.-C. *Adv. Mater. Sci. Eng.* **2014**, *2014*, 578168.
- (29) Lv, H.; Xu, X.; Sun, P.; Liu, H.; Luo, Q.; Liu, Q.; Banerjee, W.; Sun, H.; Long, S.; Li, L.; Liu, M. *Sci. Rep.* **2015**, *5*, 13311.
- (30) Beebe, J. M.; Kim, B.; Gadzuk, J. W.; Frisbie, C. D.; Kushmerick, J. G. *Phys. Rev. Lett.* **2006**, *97* (2), No. 026801.
- (31) Onofrio, N.; Guzman, D.; Strachan, A. *Nat. Mater.* **2015**, *14* (4), 440–6.
- (32) German, R. M. Chapter Seven—Thermodynamic and Kinetic Treatments. In *Sintering: from Empirical Observations to Scientific Principles*; German, R. M., Ed.; Butterworth-Heinemann: Boston, 2014; pp 183–226.
- (33) Haemori, M.; Nagata, T.; Chikyow, T. *Appl. Phys. Express* **2009**, *2*, No. 061401.
- (34) Park, J.; Lee, W.; Choe, M.; Jung, S.; Son, M.; Kim, S.; Park, S.; Shin, J.; Lee, D.; Siddik, M.; Woo, J.; Choi, G.; Cha, E.; Lee, T.; Hwang, H. In *Quantized conductive filament formed by limited Cu source in Sub-Snm era*; 2011 International Electron Devices Meeting, Dec 5–7, 2011; pp 3.7.1–3.7.4.
- (35) Chang, T.; Jo, S.-H.; Kim, K.-H.; Sheridan, P.; Gaba, S.; Lu, W. *Appl. Phys. A: Mater. Sci. Process.* **2011**, *102* (4), 857–863.
- (36) Jo, S. H.; Chang, T.; Ebong, I.; Bhadviya, B. B.; Mazumder, P.; Lu, W. *Nano Lett.* **2010**, *10* (4), 1297–301.
- (37) Shouval, H.; Wang, S.; Wittenberg, G. *Front. Comput. Neurosci.* **2010**, *4* (19), 1–19.
- (38) Song, S.; Miller, K. D.; Abbott, L. F. *Nat. Neurosci.* **2000**, *3*, 919.
- (39) Gerstner, W.; Kistler, W. M. *Spiking neuron models: Single neurons, populations, plasticity*; Cambridge University Press, 2002.