23.8 A Chip-scale Electrical Soliton Modelocked Oscillator

David S. Ricketts, Donhee Ham

Harvard University, Cambridge, MA

The generation of electrical pulses with durations in the picosecond range is an important topic in modern electronics [1]-[3]. Ultrafast time-domain metrology represents one of the most significant application spaces for these sharp pulses [1][2], since their narrow width directly translates to high temporal resolution. Two outstanding application examples of sharp pulses in time-domain metrology are their use in sampling rapidly changing electrical signals in high-speed electronics and their use as probe signals for high-resolution time-domain reflectometry.

One of the most powerful vehicles for generating sharp electrical pulses is the nonlinear transmission line (NLTL), a 1-D network of inductors and varactors (Fig. 23.8.1, top) [2][3]. This is due to the NLTL's unique ability to compress an input pulse into a sharp, spatially-confined, pulse known as a soliton. In previous NLTL works over the past 40 years, the NLTL has been almost exclusively used as a "2-port" (input + output) system, which requires an external input to generate a soliton output (See Fig. 23.8.1, top.).

Recently, however, the authors introduced a new concept, the "1-port" (output only) NLTL-based soliton oscillator [4]. This oscillator self-generates a train of periodic soliton pulses grown from ambient noise. This circuit differs significantly from the previous 2-port NLTL works, in that it is a 1-port system that does not require any external high-frequency input. This 1-port pulse-based (or mode-locked) oscillator is a self-contained system that provides improved control and pulse quality. The soliton oscillator was made possible by combining the NLTL with a special amplifier in a circular loop (Fig. 23.8.1, bottom) [4]. The first proofs-of-concept in [4] were in the form of discrete MHz prototypes, and the soliton oscillator's on-chip operation has up until now not been demonstrated.

This paper presents the realization of the soliton oscillator concept at the chip scale with GHz operating frequency. This system leverages the topology (Fig. 23.8.1, bottom) and operating principles of our previous discrete prototypes [4]. The goal of this oscillator topology is to self-generate one of the soliton circulation modes of a ring NLTL (Fig. 23.8.2, left), where the modes are created by the periodic boundary conditions. To this end the oscillator topology uses a non-inverting amplifier inserted into the ring NLTL (Fig. 23.8.1, bottom).

Unfortunately, however, this circular-loop topology can lead to an unstable soliton oscillation with significant modulations in the pulse amplitude and repetition rate (Fig. 23.8.2, right) [4]. This is because the topology not only generates the desired soliton circulation mode, but can also excite other parasitic solitons created from small perturbations (e.g., noise) or amplifier distortion. The desired and parasitic solitons have generally different amplitudes, and hence circulate in the loop at different speeds due to the solitons' amplitude-dependent velocity. This results in continual collisions between the desired and parasitic solitons, which modulates the pulse amplitude and repetition rate [4], leading to the unstable oscillation. Therefore, to achieve a stable soliton oscillation, the amplifier should, in addition to providing gain, incorporate mechanisms to prevent the growth of the parasitic solitons in steady state by 1) attenuating small perturbations and 2) reducing amplifier distortion [4].

The stability mechanisms are accomplished with the amplifier whose transfer curve is shown in Fig. 23.8.3. The transfer curve is divided into the attenuation, gain, and saturation regions. At the initial startup stage, the amplifier is biased at A in the gain region, where ambient noise is amplified to start the oscillation (Fig. 23.8.3, left). As the oscillation signal grows into a soliton train, the *dc* component of the amplifier output increases (Fig. 23.8.3, bottom), which is used to adaptively lower the amplifier bias (dashed arrow in Fig. 23.8.3, right). The reduced bias corresponds to an overall gain reduction, since a portion of the pulse enters the attenuation region. The bias point moves down on the curve until the overall gain becomes equal to the system loss, settling at steady-state bias B (Fig. 23.8.3, right). At this point, the input pulses are placed across both the attenuation and gain regions, causing small perturbations to be attenuated while maintaining gain for the main portions of the desired pulses, thereby satisfying the first stability requirement (perturbation attenuation). This threshold-dependent attenuation-gain mechanism was invented in the electrical domain [5] but has been almost exclusively used in optics, where it is known as *saturable absorption*. In addition to the perturbation attenuation, in steady state the bias (B) is low enough to keep the input soliton out of the saturation region, thereby satisfying the second stability requirement (reduced amplifier distortion). By using these amplification techniques in conjunction with the NLTL in the circular loop topology (Fig. 23.8.1, bottom), we were able to achieve stable soliton oscillations in our chip-scale oscillator. (Fig. 23.8.4 shows the stable soliton oscillations of our previous discrete prototypes in [4], further validating our stabilization approach.)

The chip-scale soliton modelocked oscillator was implemented in a CMOS integrated circuit. Figure 23.8.5 shows the schematic of the entire oscillator, where the amplifier is shown inside the dashed box. This schematic includes a more detailed description of the topology shown in Fig. 23.8.1, bottom, including the termination network, which is needed to absorb energy [4]. This termination is not ideal due to the NLTL's voltage-dependent characteristic impedance. Fortunately, however, the resulting reflections will be attenuated by the amplifier's saturable absorption mechanism.

The amplifier in Fig. 23.8.5 consists of two functionally equivalent, complementary inverting stages, one built around an NMOS transistor, M_1, and the other built around a PMOS transistor, M_2, which, when taken together, form a non-inverting amplifier. The PMOS stage functions as follows. The waveform at the amplifier output, V_Y, is sensed by the voltage divider consisting of the two resistors, R_a and R_b, and then is integrated by the R_2-C_2 low pass filter. The integrated voltage, V_2, represents a scaled *dc* component of the waveform, V_Y. This *dc* component is fed back to the gate of M_2 through the feedback resistor, R_f, to set its bias. As the *dc* level of V_Y increases, V_2 will rise with respect to ground. The increase in V_2 corresponds to a reduction in the gate-source voltage of M_2, effectively lowering its bias. A similar argument applies to the NMOS stage. Combining the two stages, the bias of the amplifier at the input is reduced as the *dc* component of V_Y increases. This overall achieves the amplifier functionality described in Fig. 23.8.3.

Figure 23.8.7 shows a micrograph of the chip-scale soliton oscillator. The IC, fabricated in 0.18μm CMOS technology, contains the amplifier and NLTL varactors (*pn* junction diodes) and is mounted on top of a glass substrate. The NLTL inductors were created by bonding gold wires back and forth between the IC and the glass substrate, which allowed for post-fabrication adjustment of the NLTL properties.

The oscillator self-started from noise, and yielded a stable soliton oscillation. Figure 23.8.6 shows the voltage signals measured at three different points on the NLTL using a real-time oscilloscope. The pulse at the amplifier output, V_Y, which is 429ps wide (FWHM), is sharpened as it propagates down the NLTL due to the soliton compression. At the eighth section on the NLTL the pulse has been compressed to 385ps, the minimum pulse width. From this point, the soliton damping [4] becomes a dominant process due to the loss in the NLTL and widens the pulse to 498ps at the amplifier input, V_X. These spatial dynamics elucidate the two competing dynamics in the oscillator: 1) the pulse sharpening due to soliton compression on the NLTL and 2) the pulse widening due to the loss on the NLTL. The soliton compression within the loop is the most interesting aspect of this oscillator, as it suggests the ability of the system to generate sharp pulses overcoming the amplifier bandwidth. Figure 23.8.6 (inset) shows the soliton oscillation measured on another sample with the smallest pulse width achieved, 293ps at a repetition rate of 1.1GHz.

With the chip-scale operation now demonstrated, the system, especially the NLTL, can be quickly scaled to a smaller size and optimized to provide significantly narrower pulse widths. It has been demonstrated that a 2-port on-chip NLTL can achieve a pulse rise time of 480fs [3]. Incorporation of such an ultrafast NLTL in our soliton modelocked oscillator will offer the possibility to self-generate a soliton pulse whose width is close to one picosecond.

Acknowledgements:
We thank R. Sullivan, L. DeVito, and S. Feindt of ADI for support; X. Li of Harvard and T. H. Lee of Stanford for suggestions; and Agilent EEsof for ADS.

References:
[1] M. Kahrs, "50 Years of RF and Microwave Sampling," *IEEE Trans. MTT*, vol. 51, no. 6, pp. 1787-1805, June, 2003.
[2] M. Rodwell et al, "Active and Nonlinear Wave Propagation Devices in Ultrafast Electronics and Optoelectronics," *Proc. IEEE*, vol. 82, no. 7, pp. 1037-1059, July, 1994.
[3] D. van der Weide, "Delta-Doped Schottky Diode Nonlinear Transmission Line for 480-fs, 3.5-V Transients," *Applied Physics Letters*, vol. 65, pp. 881-883, Aug., 1994.
[4] D. Ricketts, X. Li, and D. Ham, "Electrical Soliton Oscillator," *IEEE Trans. MTT*, Jan., 2006.
[5] C. C. Cutler, "The Regenerative Pulse Generator," *Proc. IRE*, vol. 43, no. 2, pp. 140-148, Feb., 1955.

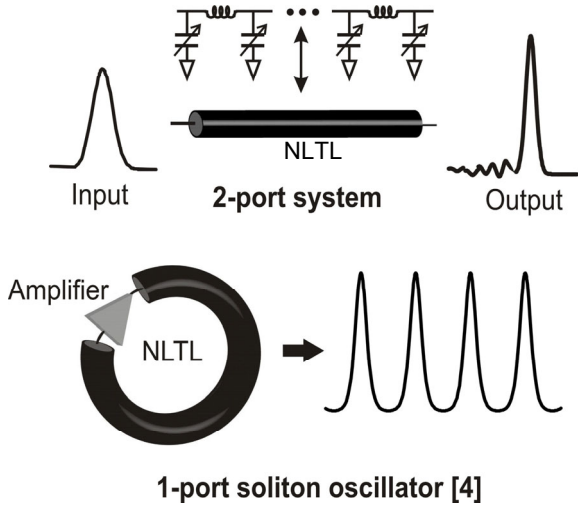

Figure 23.8.1: 2-port NLTL (top) versus 1-port soliton oscillator (bottom).

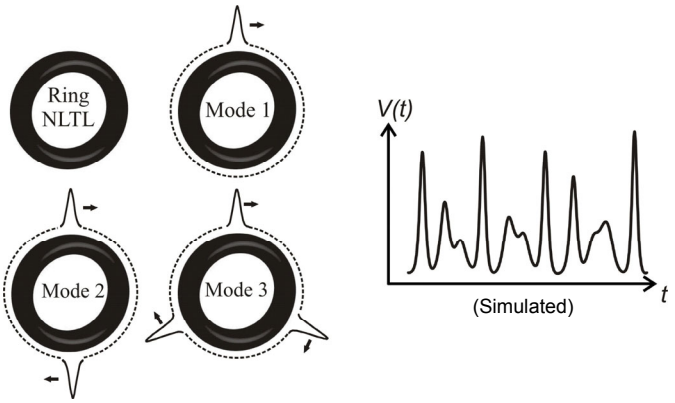

Figure 23.8.2: Soliton circulation modes (left) and oscillation instabilities (right).

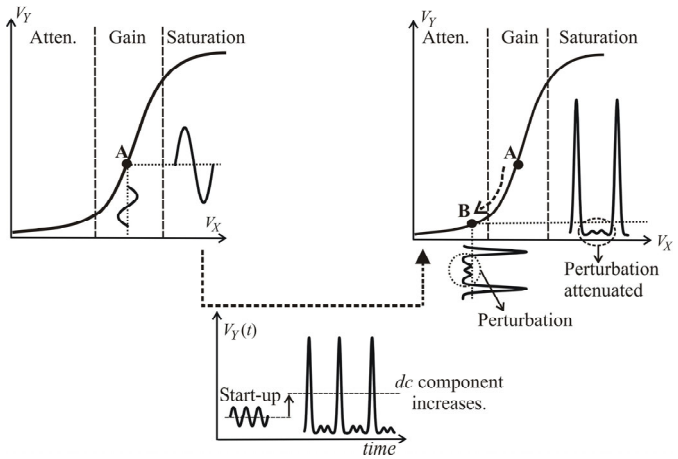

Figure 23.8.3: Stabilizing mechanisms of the amplifier.

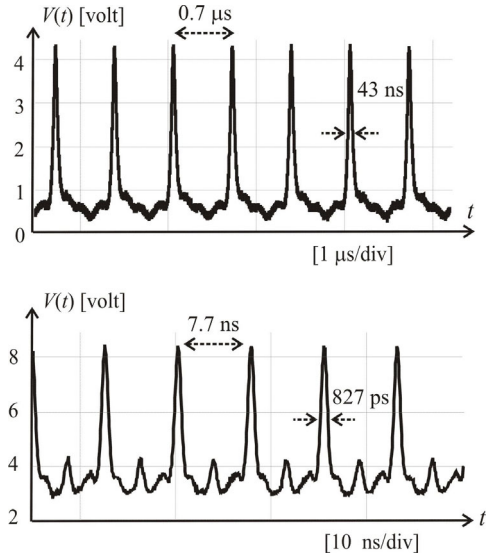

Figure 23.8.4: Stable soliton oscillation from previous discrete prototypes in [4].

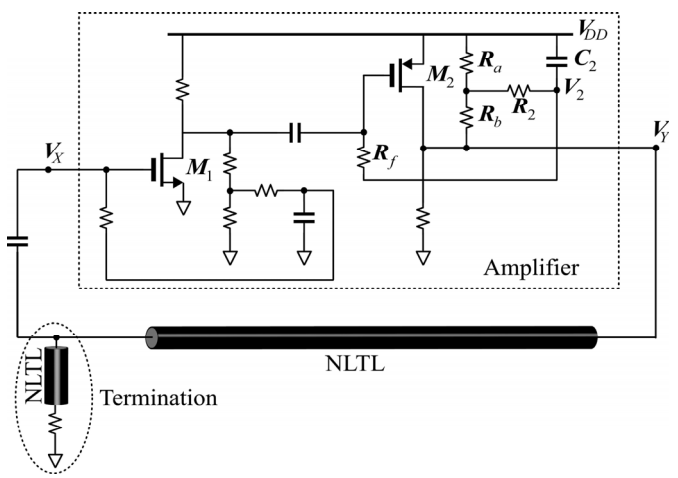

Figure 23.8.5: Schematic of the CMOS soliton oscillator.

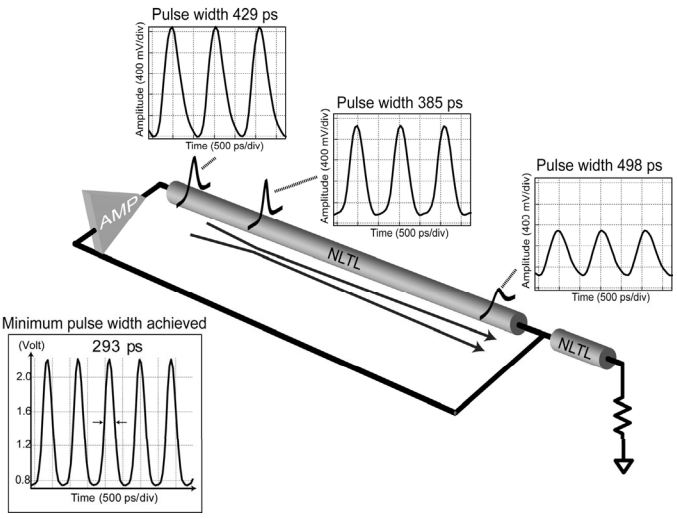

Figure 23.8.6: Measured spatial dynamics of the CMOS soliton oscillator.

Continued on Page 663

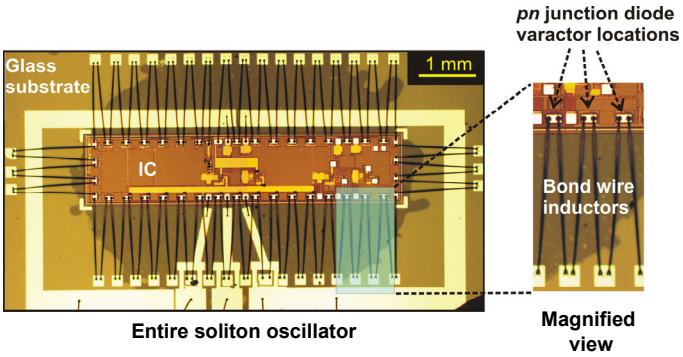

Figure 23.8.7: Micrograph of the CMOS soliton oscillator.

