Digital Acceleration of Correlation-Based Digital Background Calibration in Pipelined ADCs

Nan Sun and Donhee Ham

***Abstract*—We present here a general digital method to accelerate correlation-based digital background calibration in pipelined ADCs. The central task in correlation-based background calibration is the extraction of component mismatch information from correlated data sequences. Using an explicit frequency domain analysis, we treat the extraction process as discrete-time low pass filtering. We then show that a higher-order, variable-bandwidth filter, while adding minimal digital cost, rapidly extracts mismatch information, making calibration 18 times faster in simulation than the 1st-order, fixed bandwidth filter. The latter filter functions essentially the same as the currently widely used extraction algorithm, such as the sequential iterative algorithm or the signal averager.**

***Index Terms*—Analog-to-digital converter, pipelined analog-to-digital converter, calibration, discrete-time filter.**

I. Introduction

CORRELATION-BASED digital background calibration is being actively studied as a means to mitigate component mismatch errors in pipelined ADCs [1]–[8]. Currently, a marked drawback of correlation-based background calibration is slow convergence. In [1], a substantially fast convergence technique was reported, but it was an analog solution.

Here we propose an all-digital fast convergence technique that can be used in any correlation-based digital background calibration in pipelined ADCs. Our fast convergence technique adds no extra analog circuit, and requires minimal extra digital cost.

The central procedure in correlation-based digital background calibration is the extraction of component mismatch information from correlated data sequences. It is this extraction process that determines convergence time. The mismatch information extraction process and convergence time problem have so far been analyzed and tackled mostly in time domain [1]–[8]: in this approach, the extraction procedure is treated as a sequential, iterative algorithm [1], [2], or as time-domain averaging of correlated data sequences [3]–[8].

The same extraction process may be alternatively viewed as low pass filtering in frequency domain. The starting key to our fast convergence solution was to take this familiar, elementary notion to the next step, and to construct an explicit frequency domain picture of the extraction process. The concrete frequency domain picture thus formulated allowed us to transform the convergence problem into a discrete-time infinite impulse response (IIR) low pass filter (LPF) design problem. Our fast convergence solution followed. We substantially accelerated convergence (18 times in simulations of a 13-bit pipelined ADC) by using a higher-order, variable bandwidth IIR LPF instead of the 1st-order, fixed bandwidth IIR LPF. Here the 1st-order, fixed bandwidth filter, if viewed in time domain, functions essentially the same as the currently widely used extraction algorithm, such as the sequential iterative algorithm [1], [2] or the signal averager [3]–[8]. Our acceleration technique that changes filter order and bandwidth adds minimal digital cost.

We will now detail the development outlined above. Section II provides a frequency-domain elucidation of correlation-based digital background calibration. This provides a foundation for understanding our fast convergence technique in Section III. Simulations in Section IV confirm the validity of our technique. Throughout this report we will present our general technique in the context of capacitor mismatch errors. Extension to other nonidealities should be straightforward.

Nan Sun and Donhee Ham are with Electrical Engineering and Applied Physics, School of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138, USA (Email: nansun@seas.harvard.edu, donhee@seas.harvard.edu).

II. Frequency Domain Analysis of Correlation-based Background Calibration

This section seeks to attain the explicit frequency-domain picture of the general correlation-based digital background calibration. It will serve as a foundation for conceptualizing our fast-convergence technique presented in Section III.

We start with the abstract model of Fig. 1, for the general correlation-based digital background calibration of capacitor mismatch errors in pipelined ADCs. Detailed implementations may vary, but the model of Fig. 1 captures the essence and is generally applicable. In Fig. 1, the real ADC is separated to an ideal ADC with no capacitor mismatch, and the explicit capacitor mismatch, Δ. To understand Δ concretely, let us take an example of typical 1-bit or 1.5-bit-per-stage pipelined ADCs. In any given stage, the mismatch between a sampling capacitor C_1 and a feedback capacitor C_2 may be represented by $\Delta \equiv |C_1/C_2 - 1|$, and we can think that the model of Fig. 1 is being applied to each stage. Alternatively, we can think of Δ as what collectively represents the overall capacitor mismatch.

The calibration procedure in Fig. 1 is as follows. First, the capacitor mismatch Δ is correlated with a causal pseudo-random signal $X[n]$ ($+1$ or -1 with equal probability for $n \geq 0$; 0 for $n < 0$) and this correlation is added to the real ADC input, $V_{in}[n]$. This sum is passed through the ideal ADC. We denote the pre-calibrated digital output of the ADC as $D_{out}[n]$. As noted in Fig. 1, $D_{out}[n] = V_{in}[n] + X[n]\Delta + e[n]$, where $e[n]$ is quantization noise. Now, $D_{out}[n]$ is correlated with the same digital pseudo-random signal $X[n]$. Since $X^2[n] = u[n]$ ($u[n]$ is the unit-step function; due to causality), we attain $\Delta \cdot u[n] + X[n]V_{in}[n] + X[n]e[n]$ as the outcome of the second correlation. We will denote this signal as $\Delta_{in}[n]$:

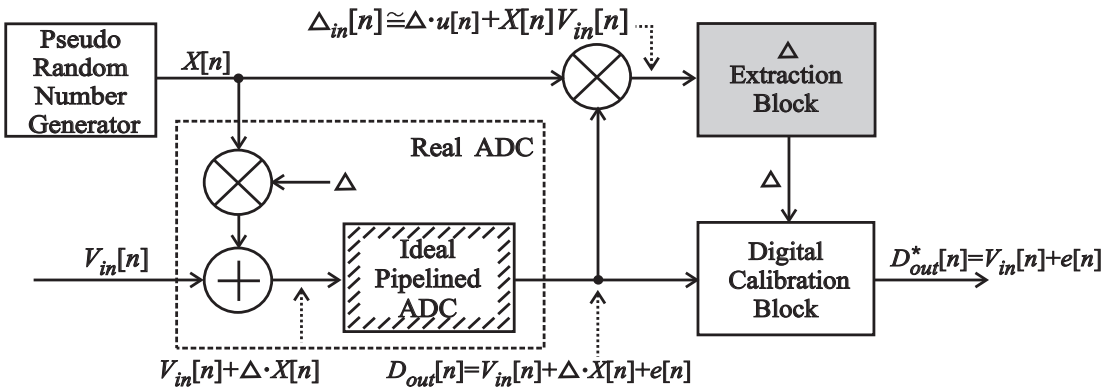

Fig. 1. Correlation-based digital background calibration.

$$\begin{aligned}\Delta_{in}[n] &\equiv \Delta \cdot u[n] + X[n]V_{in}[n] + X[n]e[n] \\ &\cong \Delta \cdot u[n] + X[n]V_{in}[n] \end{aligned} \quad (1)$$

Here we have neglected $X[n]e[n]$, for $V_{in}[n] \gg e[n]$ in any reasonably high resolution application [1].[1] $\Delta_{in}[n]$ in (1) bears the capacitor mismatch information, Δ, which, however, is obscured by the additive term, $X[n]V_{in}[n]$. The key step in the entire background calibration is to extract Δ from $\Delta_{in}[n]$, by removing the additive term. Once Δ is extracted, it can be used in a standard digital block to correct capacitor mismatch errors in $D_{out}[n]$, yielding the desired digital output, $D^*_{out}[n] = V_{in}[n] + e[n]$.

In this model, extracting Δ within a given accuracy from $\Delta_{in}[n]$ of (1) requires a certain number of samples (the index 'n' needs to run over a certain set of integers), which defines convergence time. The convergence time depends crucially on the specific extraction algorithm used. Currently, the sequential iterative method [1], [2] or certain signal averaging method [3]–[8] is used, and we in Section III propose a different method, which is the key to our fast convergence solution and is the contribution of this work. To understand how the iterative algorithm or the currently used averaging differs from our fast-convergence solution, let us first gain a frequency domain picture of $\Delta_{in}[n]$ of (1).

The Fourier transform of the first term of (1), $\Delta \cdot u[n]$, is:

$$\mathscr{F}\{\Delta \cdot u[n]\} = \Delta \left[\frac{1}{1 - e^{j\omega}} + \sum_{k=-\infty}^{\infty} \pi\delta(\omega + 2\pi k) \right] \quad (2)$$

As for the second term $X[n]V_{in}[n] \equiv Y[n]$ of (1), since it is a random process, we calculate its power spectral density (PSD) to obtain its frequency domain representation. To this end, let us first denote the autocorrelation function of $X[n]$, $V_{in}[n]$ and $Y[n]$ as $R_{XX}[m]$, $R_{VV}[m]$, and $R_{YY}[m]$, respectively. Since $X[n]$ and $V_{in}[n]$ are independent random processes, $R_{YY}[m] = R_{XX}[m] \cdot R_{VV}[m]$. Suppose $X[n]$ is a pseudo-random signal with period T: after time T, the same pattern of $X[n]$ is repeated. If T is large enough, $R_{XX}[m]$ may be modeled as:

$$\begin{aligned} R_{XX}[m] &= E\big[X[n] \cdot X[n+m]\big] \\ &\cong \frac{1}{2} \sum_{n=-\infty}^{\infty} \delta[m - nT] \end{aligned} \quad (3)$$

where $\delta[n]$ is the discrete-time delta function. This model is approximately valid, as the correlation of $X[n]$ and $X[n+m]$ is approximately[2] zero if m is not an integer multiple of T, and it is exactly one half[3] if m is an integer multiple of T and the two sequences overlap perfectly.

Let us now denote the PSD of $X[n]$, $V_{in}[n]$, and $Y[n]$ as $\Phi_{XX}(e^{j\omega})$, $\Phi_{VV}(e^{j\omega})$, and $\Phi_{YY}(e^{j\omega})$. Using Wiener-Khinchin theorem and (3), we obtain:

$$\begin{aligned} \Phi_{XX}(e^{j\omega}) &= \mathscr{F}\Big\{R_{XX}[m]\Big\} \\ &= \frac{\pi}{T} \sum_{k=-\infty}^{\infty} \delta(\omega - \frac{2\pi k}{T}), \end{aligned} \quad (4)$$

and, subsequently,

$$\begin{aligned} \Phi_{YY}(e^{j\omega}) &= \mathscr{F}\Big\{R_{XX}[m] \cdot R_{VV}[m]\Big\} \\ &= \frac{1}{2\pi} \int_{-\pi}^{+\pi} \Phi_{XX}(e^{j\theta}) \Phi_{VV}(e^{j(\omega-\theta)}) d\theta \\ &= \frac{1}{2T} \sum_{k=-\frac{T}{2}}^{\frac{T}{2}} \Phi_{VV}(e^{j(\omega - \frac{2\pi k}{T})}) \end{aligned} \quad (5)$$

The frequency domain illustrations of these results are in Fig. 2. $\Phi_{VV}(e^{j\omega})$ and $\Phi_{XX}(e^{j\omega})$ are in Fig. 2(a) and Fig. 2(b), respectively. Equation (5) indicates that $\Phi_{YY}(e^{j\omega})$ is the sum of repeatedly shifted replicas of $(1/2T) \cdot \Phi_{VV}(e^{j\omega})$, which are shown in Fig. 2(c). From this figure, we can predict that $\Phi_{YY}(e^{j\omega})$ will assume a constant value regardless of ω, as shown in Fig. 2(d). We now confirm this prediction by carrying out the summation of (5). In any practical correlation-based digital background calibration, T is large enough so that $2\pi/T$ is much smaller than the input signal bandwidth. Therefore,

[1]For a given ADC input, $e[n]$ depends on the value of $X[n]$, and hence $e[n]$ and $X[n]$ could be correlated [8]. If the correlation were strong, the omission of $X[n]e[n]$ should be reexamined, but in practical situations where $V_{in}[n]$ is a random signal, the correlation should be negligibly weak.

[2]The approximate nature originates from the "pseudo"-randomness.

[3]One half instead of one is the result of causality, i.e., $X[n] = 0$ for $n < 0$.

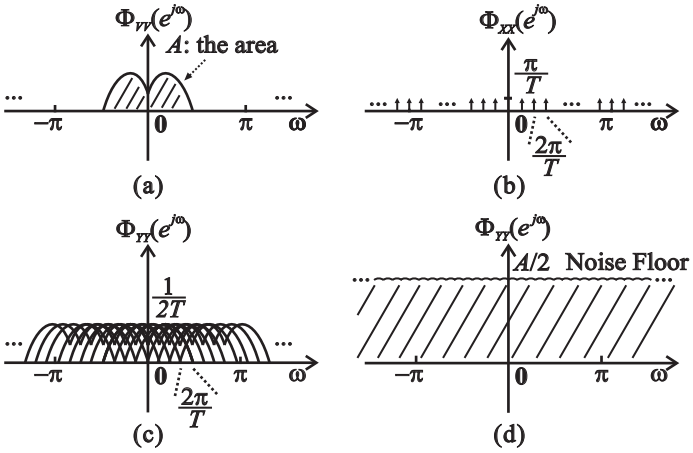

Fig. 2. PSDs of $\Phi_{VV}(e^{j\omega})$, $\Phi_{XX}(e^{j\omega})$, and $\Phi_{YY}(e^{j\omega})$.

$\Phi_{YY}(e^{j\omega})$ of (5) may be rewritten as

$$\begin{aligned}\Phi_{YY}(e^{j\omega}) &\simeq \frac{1}{2}\int_{\omega-\pi}^{\omega+\pi}\Phi_{VV}(e^{j\theta})d\theta \\ &= \frac{1}{2}\int_{-\pi}^{\pi}\Phi_{VV}(e^{j\theta})d\theta \\ &= \frac{1}{2}\Big[\text{Energy of input } V_{in}[n]\Big] \qquad (6)\end{aligned}$$

where we have resorted to the fact that $\Phi_{VV}(e^{j\omega})$ has a period of 2π in obtaining the second line.

The analysis above leads to a few meaningful interpretations of the second term $Y[n] = X[n]V_{in}[n]$ of $\Delta_{in}[n]$ in (1), for any practical, large-enough value of T:

1) $\Phi_{YY}(e^{j\omega})$ is not a function of frequency, that is, $Y[n] = V_{in}[n]X[n]$ is a discrete-time white noise. See Fig. 2(d).
2) $\Phi_{YY}(e^{j\omega})$ is half the input signal energy. Therefore, an input signal $V_{in}[n]$ with larger energy leads to a higher white noise floor in Fig. 2(d), making it harder to extract Δ from $\Delta_{in}[n]$ of (1): a longer convergence time is required to average out the larger noise. This also explains why foreground calibration is much faster than background calibration. In foreground calibration, $V_{in}[n] = 0$, and hence the noise floor is zero, so we need much less time for convergence.
3) The noise floor level $\Phi_{YY}(e^{j\omega})$ has no dependence on T. Increasing pseudo-random signal period T will *not* help reduce noise floor.

Results 1) and 2) above were also insightfully conveyed in [1], but qualitatively with no explicit Fourier analysis.[4] As we will see shortly, the way we fully utilize these results to transform the convergence problem into a filter design problem also differentiates our approach.

Fig. 3 shows the overall frequency domain picture of $\Delta_{in}[n]$, by combining the white noise $\sqrt{\Phi_{YY}(e^{j\omega})}$ and the mismatch information signal $\mathscr{F}\{\Delta \cdot u[n]\}$ of (2). The mismatch information signal amplitude is equal to the noise amplitude at ω_0. Since the noise, directly affected by $V_{in}[n]$, is rather strong compared to the mismatch information signal,

[4]The qualitative treatment in [1] led to a misconception that increasing T would reduce noise floor, which is wrong according to Result 3).

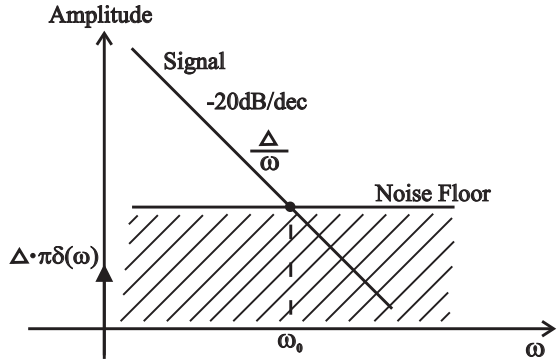

Fig. 3. Frequency-domain representation of $\Delta_{in}[n]$ of (1). Log scale.

ω_0 is quite small. Therefore, in the vicinity of ω_0, $\omega \ll 1$ and we can model $\mathscr{F}\{\Delta \cdot u[n]\}$ of (2) as a -20 dB/dec line, for $\Delta/(1-e^{j\omega}) \cong -\Delta/(j\omega)$.

From the analysis above and Fig. 3, we see the function of Δ-extraction block of Fig. 1 is to extract Δ out of the noise floor in frequency domain. We have just transformed the problem of designing a faster Δ-extraction block into a filter design problem. As mentioned earlier, convergence time is determined by the Δ-extraction block. Therefore, attaining faster convergence within a given calibration accuracy is to design a discrete-time LPF with a bandwidth high enough to settle fast (for convergence time) but low enough to reject much of the white noise (for accuracy). Building on this filter design notion, we in the next section will explain how our fast convergence solution works.

But before moving on, we would like to further shed light on the correctness of the filter picture, by proving that the sequential iterative method for Δ-extraction used in [1], [2] is equivalent to the 1st-order IIR LPF. The iterative method can be generally modeled as:

$$\Delta^*[n+1] = \Delta^*[n] + \varepsilon(\Delta_{in}[n] - \Delta^*[n]) \qquad (7)$$

Here $\Delta^*[n]$ denotes the estimated capacitor mismatch after the n-th iteration and ε denotes the iteration step size. By plugging $\Delta_{in}[n]$ of (1) into the equation above, we obtain

$$\Delta^*[n+1] = \Delta^*[n] + \varepsilon(\Delta - \Delta^*[n]) + \varepsilon X[n]V_{in}[n] \qquad (8)$$

$\Delta - \Delta^*[n]$ can be regarded as the correction term of every iteration, which makes the next iterative value $\Delta^*[n+1]$ closer to the real capacitor mismatch Δ. If $\Delta^*[n] < \Delta$, $\Delta - \Delta^*[n] > 0$, and a larger $\Delta^*[n+1]$ results in the next iteration. Similarly, this algorithm works for $\Delta^*[n] < \Delta$. Consequently, starting from an initial value $\Delta[0] = 0$, $\Delta[n]$ will gradually converge to Δ. By setting ε to be sufficiently small, $\varepsilon X[n]V_{in}[n]$ will eventually appear as a small random perturbation.

The time-domain picture above can be re-examined in frequency domain. If we consider $\Delta_{in}[n]$ and $\Delta^*[n]$ as the input and output of the Δ-extraction block, by applying z-transform to (7), we obtain:

$$\frac{\Delta^*(z)}{\Delta_{in}(z)} = \frac{\varepsilon}{z-1+\varepsilon} \qquad (9)$$

The iterative Δ-extraction process is no more than a 1st-order IIR LPF with passband bandwidth ε. The iterative algorithm

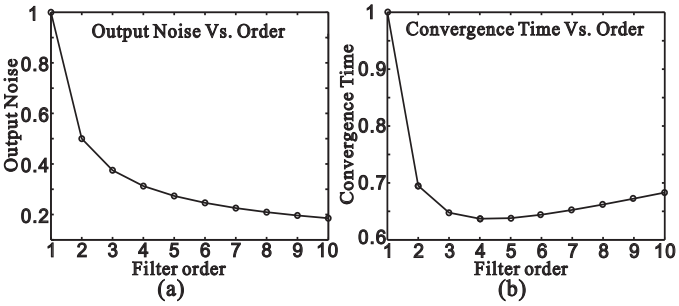

Fig. 4. (a) LPF output noise (normalized to the 1st-order value) vs. LPF order. The LPF's bandwidth is fixed. (b) Convergence time (normalized to the 1st-orde value) vs. LPF order. Total LPF output noise energy is fixed.

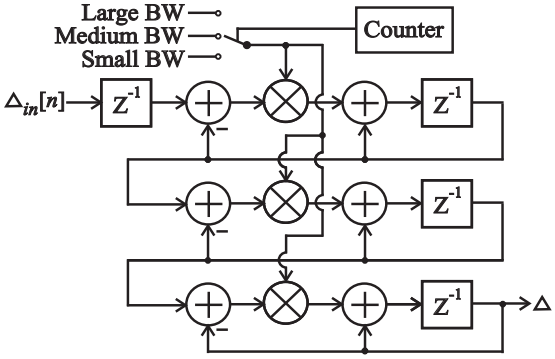

Fig. 5. 3rd-order discrete-time IIR LPF with a variable bandwidth scheme.

lets $\Delta_{in}[n]$, which contains Δ and the noise term, go through the 1st-order IIR LPF to extract Δ by filtering out the noise.

The analysis above further supports our picture that the design of the Δ-extraction block is essentially a filter design problem. From now on, we will treat the Δ-extraction block exclusively as a discrete-time LPF, and will move on to discuss how we design the LPF to achieve fast convergence.

III. Fast Convergence Technique

Based on the frequency domain picture of $\Delta_{in}[n]$ in Fig. 3, we clearly see the trade-off in deciding the LPF bandwidth. If the bandwidth is small, the convergence will be accurate rejecting more noise, but it will take long for calibration to converge. If the bandwidth is large, convergence will be fast, but more noise is filtered in, undermining calibration accuracy. Convergence time trades off with calibration accuracy via the bandwidth. In light of this observation, it is easy to appreciate the disadvantage of the 1st-order LPF (both the iterative algorithm [1], [2] and the averager [3]–[8]). Filter order has been fixed and bandwidth is the only design parameter to play with, and the tradeoff is directly faced. To satisfy a required accuracy, the LPF bandwidth is set small enough, resulting in a long convergence time. Such design constraint becomes more troublesome in high resolution applications where calibration accuracy requirement is stringent.

Our fast convergence technique is enabled by relaxing the tradeoff between convergence time and accuracy. This is achieved by incorporating two features in the discrete-time IIR LPF, as described in the following two subsections.

A. Higher-Order Discrete-Time IIR LPF

In the iterative extraction algorithm [1], [2] or averaging algorithm [3]–[8], the effective filter order was fixed to 1. Filter order, however, is another design parameter one can exploit in the design of discrete-time IIR LPFs. This we do, and it relaxes the tradeoff between convergence time and accuracy: as seen shortly, for a given accuracy, LPFs with order 3 to 5 extract Δ faster than 1st-order LPFs.

Let us first note that for the same bandwidth a higher-order LPF rejects more noise, because a higher order corresponds to a steeper frequency response at the falling edge. This property is observed in our numerical analysis of a discrete-time filter in Fig. 4(a): for a fixed bandwidth, as filter order increases, total noise energy at the LPF output decreases. For example, total noise energy at the output of a 3rd-order LPF is less than 40% of that of a 1st-order LPF.

Therefore, when the target calibration accuracy is given, that is, when the LPF output noise energy is specified, a higher-order LPF can accommodate a wider bandwidth, leading to faster convergence. This property is seen in our another numerical analysis of a discrete time filter in Fig. 4(b): for the fixed LPF output noise energy, as filter order increases to 3$\sim$5, the bandwidth is increased and the convergence time is reduced by more than 35%, as compared to the 1st-order LPF. Here the convergence time is defined as the number of samples required for ENOB to reach within 1 bit of the ideal value. As the filter order is increased beyond 5, while bandwidth continues to be increased to maintain the same output noise energy, the convergence time slightly goes up because the signal itself is now rejected quite noticeably while the bandwidth increase is not as substantial as in the lower order cases. Hence an optimal filter order would be 3$\sim$5.

Increasing digital filter order to 3$\sim$5 incurs minimum digital cost: see Fig. 5 for the 3rd-order IIR LPF. A higher order filter will not cause instability, for the calibration in Fig. 1 is done in an open loop.

B. Bandwidth Switching in the Discrete-Time IIR LPF

In the foregoing subsection, introducing the filter order as another design parameter relaxed the tradeoff between convergence time and accuracy: a higher order decreased convergence time for a given accuracy. Now we introduce another way of relaxing the tradeoff, use of a larger bandwidth during the initial calibration transient and a smaller bandwidth near and during the final convergence (steady-state).

This variable bandwidth technique is based on the notion that convergence speed matters only during transient, while convergence accuracy matters only during steady state. During the initial calibration phase, in order to achieve faster convergence, a larger bandwidth is used. Although more noise is filtered in due to the larger bandwidth, during this early phase of calibration, accuracy is no concern. As convergence is approached, bandwidth is switched to a smaller value to reduce steady-state convergence errors. By using this adaptive bandwidth scheme, we circumvent the tradeoff, substantially reducing convergence time for a given accuracy.

Similar variable bandwidth schemes are widely used in other types of circuits, notably, in the design of phase-locked loops

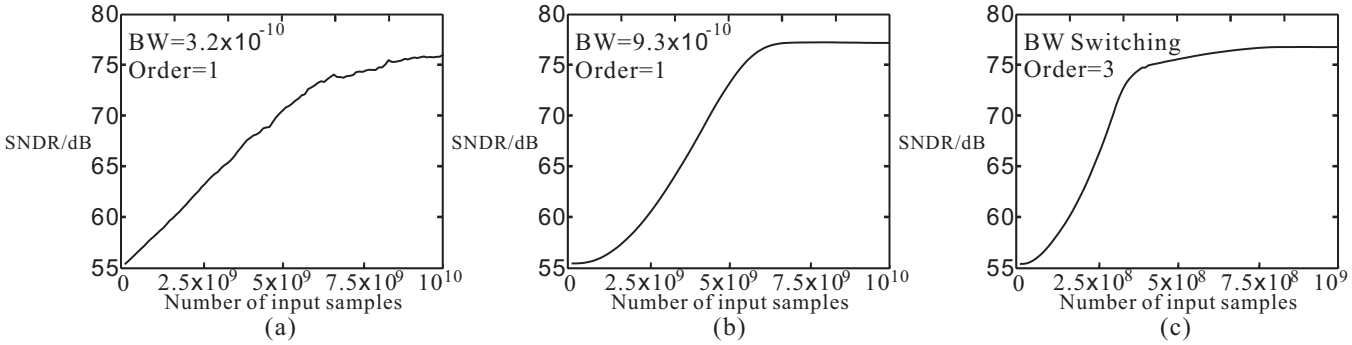

Fig. 6. Simulated convergence transients for a 13-bit pipelined ADC, for varying LPF bandwidths and orders.

[9], [10]. We later found a limited number of publications in which the variable bandwidth scheme was also used for digital background calibration of ADCs [11]–[13]. This report lays a foundation of the technique, viewing it from the systematic frequency-domain angle.

The bandwidth switching can be implemented at low cost in discrete-time filters by altering multiplication coefficients, as shown in Fig. 5 for a 3rd-order LPF example. The rest extra cost is simple combinational logic gates and a counter to determine bandwidth switching times.

IV. Simulation

Our fast convergence technique can be applied to any correlation-based background calibration in pipelined ADCs. To demonstrate the validity of our technique, we apply it to our newly proposed correlation-based background calibration [14]. A 13-bit pipelined ADC consisting of 12 1.5-bit stages is used. Behavioral simulations are carried out in MATLAB assuming random capacitor mismatch ($\sigma = 0.5\%$) in each stage. First 4 stages are calibrated in parallel using the same calibration technique of [14]. Each of the 4 stages has its own IIR LPF and pseudo-random number generator, whose period T is 2^{14}. The input signal is a random signal with full swing.

Fig. 6 shows simulated convergence transients with varying orders and bandwidths of the IIR LPF. The order and bandwidth of the LPF for Fig. 6(a) are 1 and 3.2×10^{-10}, respectively, and the convergence time (as stated earlier, we define convergence time as the number of samples needed for ENOB to reach within 1 bit of the ideal value) is 7.2×10^9. The order of the LPF for Fig. 6(b) is 3, and to keep the same output noise energy (same accuracy) as in the 1st-order LPF, the bandwidth is increased to 9.3×10^{-10}. Convergence time is accordingly reduced to 5.2×10^9, enhancing convergence speed by 1.4 times, as compared to the 1st-order LPF.

The order of the LPF for Fig. 6(c) is 3. We here apply the variable bandwidth scheme. The bandwidth is 1.5×10^{-8} when the number of input samples is less than 4×10^8, and it is switched to 3.7×10^{-9} afterwards, and finally switched to 9.3×10^{-10} after the number of input samples reaches 8×10^8. The initial bandwidth is much larger than the case of Fig. 6(a), but the final, reduced bandwidth is such that the output noise energy in the final calibration stage is the same as in the case of Fig. 6(a). The convergence time is 3.9×10^8: for the given accuracy, our technique combining a higher-order LPF with the variable bandwidth scheme speeds up convergence by 18 times, in comparison to the 1st-order, fixed-bandwidth LPF, which shares the same characteristics with the currently used extraction algorithms [1]–[8]). This attests to the validity of the proposed technique. The bandwidth values and their switching times used here are for proof of concept: they can be further optimized for even faster convergence.

V. Conclusion

The digital fast-convergence technique presented here as a low cost means of accelerating correlation-based background calibration was enabled by a change of view on the mismatch information extraction process (central step in correlation-based digital background calibration) from time-domain to frequency-domain angle. This paved a way to treat the design of the mismatch extraction algorithm as a filter design problem. Subsequently, designing a higher-order filter incorporating a variable bandwidth scheme led to fast convergence.

References

[1] J. Li and U. Moon, "A background calibration techniques for multi-stage pipelined ADCs with digital redundancy," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 9, pp. 531-538, Sept. 2003.

[2] M. Taherzadeh-Sani and A. A. Hamoui, "Digital background calibration of capacitor-mismatch errors in pipelined ADCs," *IEEE Trans. Circuits Syst. II, Brief Papers*, vol. 53, no. 9, pp. 966-970, Sept. 2006.

[3] R. Jewett, K. Poulton, K. Hsieh, and J. Doernberg, "A 12-b 128M samples/s ADC with 0.05LSB DNL," *Proc Int. Solid-State Circuits Conf.*, pp. 138-139, Feb. 1997.

[4] J. Ming and S. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE J. Solid-Sate Circuits*, vol. 36, no. 9, pp. 1489-1497, Oct. 2001.

[5] I. Galton, "Digital cancellation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 185-196, Mar. 2000.

[6] E. Siragusa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2126-2138, Dec. 2004.

[7] K. El-Sankary and M. Sawan, "A digital blind background capacitor mismatch calibration for pipelined ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 10, pp. 507-510, Oct. 2004.

[8] A. Panigada and I. Galton, "Digital background correction of harmonic distortion in pipelined ADCs," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 53, no. 9, pp. 1885-1895, Sept. 2006.

[9] Crowley, "Phase locked loop with variable gain and bandwidth," U.S. Patent 4,156,855, May 29, 1979.

[10] K. Woo, Y. Liu, E. Nam, and D. Ham, "Fast-lock hybrid PLL combining fractional-N and integer-N modes of differing bandwidths," *IEEE J. Solid-State Circ.*, vol. 43, no. 2, pp. 379-389, Feb. 2008.

[11] K. W. Hsueh, Y. K. Chou, Y. H. Tu, Y F. Chen, Y. L. Yang, and H. S. Li, "A 1V 11b 200MS/s pipelined ADC with digital background calibration in 65nm CMOS," *IEEE Solid State Circ. Conf. Digest of Technical Papers* pp. 546-547, 2008.

[12] J. Li, G. Ahn, D. Chang, and U. Moon, "A 0.9-V 12-mW 5-MSPS algorithmic ADC with 77-dB SFDR," *IEEE J. Solid-State Circ.* vol. 40, no. 4, pp. 960-969, April 2005. Page(s):960 - 96

[13] D. Fu, K. Dyer, S. H. Lewis, and P. J. Hurst, "A digital background calibration technique for time-interleaved analog-to-digital converters," *IEEE J. Solid-State Circ.* , vol. 33, no. 12, pp. 1904-1911, Dec. 1998.

[14] N. Sun, H.-S. Lee, and D. Ham, "Digital background calibration in pipelined ADCs using commutated feedback capacitor switching," *IEEE Transaction on Circuits and Systems II*, 2008 (in press).