A 200 x 256 Image Sensor Heterogeneously Integrating a 2D Nanomaterial-Based Photo-FET Array and CMOS Time-to-Digital Converters

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The CMOS image sensor, which incorporates a silicon photodiode array and a signal processor on a chip, or in a multi-die stack, has become an indispensable part of our daily lives. While its dominance in digital image capture will foreseeably continue, research with future outlooks is actively searching for new optoelectronic devices, alternative to silicon photodiodes, to place on the CMOS signal processor. Two-dimensional (2D) semiconducting materials, in particular, atomically thin transition metal dichalcogenide (TMD) monolayers—which are one of the most actively researched solid-state materials—are especially promising candidates for these applications [1,2]. The vision arises from the fact that TMD monolayer crystals of different chemical compositions exhibit different bandgaps, or different absorption wavelengths from infrared to visible, and that these atom-thick crystals with differing bandgaps can, in principle, be van der Waals stacked to produce diverse spectral sensitivities beyond what is possible with conventional CMOS image sensors. Despite this vision, however, TMD arrays, such as those made from MoS2 optoelectronic devices (photo-FETs), have been limited to 32 x 32 thus far [3], and have not been integrated on CMOS signal processing chips; graphene was integrated with CMOS electronics, but this semimetal uses additional layers, such as quantum dots, for light absorption [4].

Here we present a 256 (H) x 200 (V) image sensor, which heterogeneously integrates a MoS2 photo-FET array on a multichannel CMOS time-to-digital converter (TDC) circuit. It not only increases the TMD array integration scale by 50 times from the state-of-the-art [3], but also does so on a CMOS integrated circuit (IC). The MoS2 photo-FET in any given pixel converts an incoming light into a photocurrent, and this photocurrent is read out by the underlying CMOS TDC through conversion to a proportional pulse width or frequency.

Figure 12.2.1, left, shows the cross-section schematic of a pixel, as well as its micrograph (top view). A large-area MoS2 monolayer grown via metal organic chemical vapor deposition (MOCVD) is placed on the CMOS planarized surface of the CMOS IC and patterned with photolithography. Relevant top metal parts of the IC are exposed and then contacted to the MoS2 monolayer to form a photo-FET with gate, source, and drain nodes defined. The gates of all the MoS2 photo-FETs are connected together across the array, as are their sources. On the other hand, the drain nodes of the MoS2 photo-FETs are multiplexed row-wise to the CMOS IC to measure individual drain (photo) currents. Figure 12.2.1, top right, shows the measured transfer curve (I_D vs. V_G) of a MoS2 photo-FET when dark and under illumination with a light intensity of 460W/m2, with the gate voltage swept from -5 to 5 V. The average dark current is 670A due to the biasing of the photocurrent, and the maximum bright current is 38nA.

In the PWM mode, CINT is initially reset to the voltage VRESET. Upon light illumination, the photocurrent through the drain of the MoS2 photo-FET in a given pixel discharges CINT, and a counter records the total number of clock cycles (tPWL) until the voltage across CINT reaches a threshold (VREF, where VREF < VRESET). Consequently, a brighter input—and thus, a larger photocurrent—will generate a smaller tPWL. A desired integration time (ttot) sets the maximum measurement time, after which CINT is refreshed to VRESET and the measurement starts anew for the next pixel. This PWM mode fully accommodates the measured 76dB bright/dark operating range of the MoS2 pixels. The total measurement range (minimum to maximum drain current) spanned by the combination of CINT (1-to-333pF) and tPWL is 122.5dB.

In the PFM mode, a delay block (tDELAY = 50 to 150ns) is connected to the comparator output to generate an automatic reset signal (with duration tRELEASE) for the readout circuit when the voltage across CINT reaches VREF. The output of the readout now becomes a sequence of pulses within a fixed time window, which is defined by the total block delay. A larger photocurrent will generate a higher frequency pulse train, and vice versa. The PFM mode allows for smaller charging capacitances, including a disconnected CINT (i.e., using the parasitic capacitance at the comparator for fastest readout), and for a higher overall current range than the PWM mode. The maximum measurable photocurrent in this mode is limited by tDELAY + tRELEASE = 54ns.

Figure 12.2.2 shows measurement curves for the TDC readout circuits in both PWM and PFM modes, where we have used an on-chip calibration current source (in lieu of the photocurrent) to characterize the linearity of the PWM and PFM modes. The calibration current (ICAL) source is swept, and the response of the TDC in each readout mode is recorded. Figure 12.2.4 demonstrates the PWM and PFM linearity for the on-chip calibration current ranging from ~70nA to ~70μA. By selecting a larger CINT, this linear readout range is shifted down to the pA-nA scale of pixel photocurrents during imaging.

Figure 12.2.5 shows an example image capture of the "Cameraman" picture using our 2D-CMOS heterogeneous image sensor. The small vertical lines seen in the upper right corner of the image stem from imperfections in the transfer of MoS2 at the pixel level—these can be ameliorated with improved fabrication techniques. The image can be further improved by calibrating out the optical memory properties (so-called persistent photoconductivity) exhibited by the 2D semiconductor. Nonetheless, this image has the largest singular frame size using TMDs to date. Figure 12.2.6 shows a device comparison table to state-of-the-art sensors using 2D materials. Notably, the state-of-the-art device with CMOS integration [4] does not feature on-chip digitization, and instead relies on an external ADC. In contrast, this work demonstrates both 2D optoelectronics, as well as a fully integrated digital readout.

Figure 12.2.7 shows the die micrograph of the composite sensor. The IC is fabricated in UMC 0.18μm technology. In each pixel region the IC accommodates a 30μm x 30μm photo-FET. Unit test devices at the top of the chip are used for characterizing single phototransistor behavior. Because the select logic fits under each pixel pad set, the fill factor within the array is 51.4%.

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References:
Figure 12.2.1: MoS₂/CMOS pixel stackup, micrograph, and MoS₂ pixel transfer curve for dark and illuminated states.

Figure 12.2.2: Chip Floorplan.

Figure 12.2.3: Device row schematic, showing connected column devices and readout circuits and waveforms for PWM and PFM measurement modes.

Figure 12.2.4: Readout circuit digital output for PWM and PFM operating modes during ID sweep from on-chip calibration circuit.

Figure 12.2.5: “Cameraman” Image Captured by 2D MoS₂ Image Sensor.

Figure 12.2.6: Device Comparison Table.

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<td>CMOS</td>
<td>0.18 (\mu)m</td>
<td>0.5 (\mu)m</td>
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<td>No</td>
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<tr>
<td>ASIC</td>
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<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Array Size</td>
<td>256 x 200</td>
<td>388 x 288</td>
<td>32 x 32</td>
<td>12 x 12 (^{(1)})</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>30 (\mu)m x 50 (\mu)m</td>
<td>35 (\mu)m x 35 (\mu)m</td>
<td>50 (\mu)m x 50 (\mu)m</td>
<td>300 (\mu)m x 300 (\mu)m</td>
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<tr>
<td>Material</td>
<td>MoS₂</td>
<td>Graphene Quantum Dot</td>
<td>MoS₂</td>
<td>MoS₂</td>
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<tr>
<td>Readout Integration</td>
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<td>Partial (Off-Chip ADC)</td>
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<td>No</td>
</tr>
<tr>
<td>Pixel Terminals</td>
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<td>2</td>
<td>3</td>
<td>3</td>
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<tr>
<td>On-Chip Resolution (bits)</td>
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<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Dynamic Range (dB)</td>
<td>76 (^{(2)})</td>
<td>55</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Effective imaging area

\(^{(2)}\) Limited by pixel on/off ratio
Figure 12.2.7: Chip micrograph.