12.2 A 200 x 256 Image Sensor Heterogeneously Integrating a 2D Nanomaterial-Based Photo-FET Array and CMOS Time-to-Digital Converters

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The CMOS image sensor, which incorporates a silicon photodiode array and a signal processor on a chip, or in a multi-die stack, has become an indispensable part of our daily lives. While its dominance in digital image capture will foreseeably continue, research with future outlooks is actively searching for new optoelectronic devices, alternative to silicon photodiodes, to place on the CMOS signal processor. Two-dimensional (2D) semiconducting materials, in particular, atomically thin transition metal dichalcogenide (TMD) monolayers—which are one of the most actively researched solid-state materials—are especially promising candidates for these applications [1,2]. The vision arises from the fact that TMD monolayer crystals of different chemical compositions exhibit different bandgaps, or different absorption wavelengths from infrared to visible, and that these atom-thick crystals with differing bandgaps can, in principle, be van der Waals stacked to produce diverse spectral sensitivities beyond what is possible with conventional CMOS image sensors. Despite this vision, however, TMD arrays, such as those made from MoS_2 optoelectronic devices (photo-FETs), have been limited to 32 x 32 thus far [3], and have not been integrated on CMOS signal processing chips; graphene was integrated with CMOS electronics, but this semimetal uses additional layers, such as quantum dots, for light absorption [4].

Here we present a 256 (H) x 200 (V) image sensor, which heterogeneously integrates a MoS_2 photo-FET array on a multichannel CMOS time-to-digital converter (TDC) circuit. It not only increases the TMD array integration scale by 50 times from the state-of-the-art [3], but also does so on a CMOS integrated circuit (IC). The MoS_2 photo-FET in any given pixel converts an incoming light into a photocurrent, and this photocurrent is read out by the underlying CMOS TDC through conversion to a proportional pulse width or frequency.

Figure 12.2.1, left, shows the cross-section schematic of a pixel, as well as its micrograph (top view). A large-area MoS_2 monolayer grown via metal organic chemical vapor deposition (MOCVD) is placed on the CMP-planarized surface of the CMOS IC and patterned with photolithography. Relevant top metal parts of the IC are exposed and then contacted to the MoS_2 monolayer to form a photo-FET with gate, source, and drain nodes defined. The gates of all the MoS_2 photo-FETs are connected together across the array, as are their sources. On the other hand, the drain nodes of the MoS_2 photo-FETs are multiplexed row-wise to the CMOS IC to measure individual drain (photo) currents. Figure 12.2.1, top right, shows the measured transfer curve (I_D vs. V_{GS}) of a MoS_2 photo-FET when dark and under illumination with a light intensity of 460W/m^2, with the gate voltage swept from -5 to 5 V. The average dark current is 670fA due to the biasing of the photo-FET, and the maximum bright current is 38nA. The maximum photoelectric on/off ratio (bright vs. dark) is 76dB. Figure 12.2.1, bottom right, shows the photo-current response of a MoS_2 photo-FET for varied illumination intensity.

Figure 12.2.2 shows the floorplan of the underlying CMOS IC, which comprises an array of 51,200 pixel circuits in the center and 200 row-wise TDCs, which are split into two 100-row sections on each side of the chip. Each pixel circuit comprises a switch to a photo-FET drain and a switch to a metal-insulator-metal (MIM) capacitor. Each TDC is multiplexed to the 256 drain switches in its row. The digitized TDC outputs are read out serially through two 12b output banks.

Figure 12.2.3 shows a TDC schematic, and its two readout modes, namely, pulse-width modulation (PWM) and pulse-frequency modulation (PFM). The selection between these two configurations is handled by a shift register-based memory block. Both of these modes depend on cyclical charging and discharging of a tunable capacitor (C_P) integrated within each TDC, whose value determines the maximum integration charge. To extend the measurement range to smaller currents, the MIM capacitors distributed across the connected pixel circuits can be connected in parallel to C_P to add an additional 256pF of integration capacitance. In addition, to each TDC we add a programmable gain transimpedance amplifier, allowing for the direct measurement of the pre-digitization analog voltage that connects to the pixel drain switches.

In the PWM mode, C_P is initially reset to voltage V_{INT}. Upon light illumination, the photocurrent through the drain of the MoS_2 photo-FET in a given pixel discharges C_P, and a counter records the total number of clock cycles (n_{CLK}), until the voltage across C_P reaches a threshold (V_{REF}, where $V_{REF} < V_{INT}$). Consequently, a brighter input—and thus, a larger photocurrent—will generate a smaller n_{CLK}. A desired integration time (t_{INT}) sets the maximum measurement time, after which C_P is refreshed to V_{INT} and the measurement starts anew for the next pixel. This PWM mode fully accommodates the measured 76dB bright/dark operating range of the MoS_2 pixels. The total measurement range (minimum to maximum drain current) spanned by the combination of C_P (1-to-333pF) and t_{INT} is 122.5dB.

In the PFM mode, a delay block (t_{DELAY} = 50 to 150ns) is connected to the comparator output to generate an automatic reset signal (with duration t_{RESET}) for the readout circuit when the voltage across C_P reaches V_{REF}. The output of the readout now becomes a sequence of pulses within a fixed time window, which is defined by the total block delay. A larger photocurrent will generate a higher frequency pulse train, and vice versa. The PFM mode allows for smaller charging capacitances, including a disconnected C_P (*i.e.*, using the parasitic capacitance at the comparator for fastest readout), and for a higher overall current range than the PWM mode. The maximum measurable photocurrent in this mode is limited by $t_{DELAY} + t_{RESET}$ = 54ns.

Figure 12.2.4 shows measurement curves for the TDC readout circuits in both PWM and PFM modes, where we have used an on-chip calibration current source (in lieu of the photocurrent) to characterize the linearity of the PWM and PFM modes. The calibration current (I_{CAL}) source is swept, and the response of the TDC in each readout mode is recorded. Figure 12.2.4 demonstrates the PWM and PFM linearity for the on-chip calibration current ranging from ~70nA to ~70μA. By selecting a larger C_P, this linear readout range is shifted down to the pA-nA scale of pixel photocurrents during imaging.

Figure 12.2.5 shows an example image capture of the "Cameraman" picture using our 2D-CMOS heterogeneous image sensor. The small vertical lines seen in the upper right corner of the image stem from imperfections in the transfer of MoS_2 at the pixel level – these can be ameliorated with improved fabrication techniques. The image can be further improved by calibrating out the optical memory properties (so-called persistent photoconductivity) exhibited by the 2D semiconductor. Nonetheless, this image has the largest singular frame size using TMDs to date. Figure 12.2.6 shows a device comparison table to state-of-the-art sensors using 2D materials. Notably, the state-of-the-art device with CMOS integration [4] does not feature on-chip digitization, and instead relies on an external ADC. In contrast, this work demonstrates both 2D optoelectronics, as well as a fully integrated digital readout.

Figure 12.2.7 shows the die micrograph of the composite sensor. The IC is fabricated in UMC 0.18μm technology. In each pixel region the IC accommodates a 30μm x 30μm photo-FET. Unit test devices at the top of the chip are used for characterizing single phototransistor behavior. Because the select logic fits under each pixel pad set, the fill factor within the array is 51.4%.

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References:
[1] H. Tian et al., "Optoelectronic devices based on two-dimensional transition metal dichalcogenides". Nano Res., 9, pp. 1543–1560 (2016).
[2] P. Ajayan, P. Kim, and K. Banerjee, "Two-dimensional van der Waals materials", Physics Today, 69, 9, 38, Sept. 2016.
[3] H. Jang et al., "Atomically Thin Optoelectronic Machine Vision Processor", Adv. Mater., 32, 2002431, July 2020.
[4] S. Goossens et al., "Broadband image sensor array based on Graphene–CMOS integration," Nat. Photonics, 11, pp. 366–371, May 2017.
[5] C. Choi et al., "Human eye-inspired soft optoelectronic device using high-density MoS2-graphene curved image sensor array", Nat. Commun., 8, 1664 (2017).

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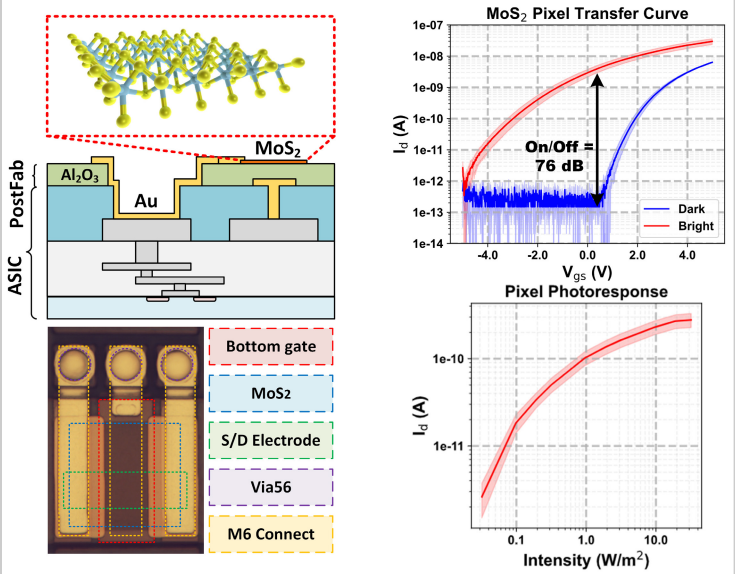

Figure 12.2.1: MoS_2/CMOS pixel stackup, micrograph, and MoS_2 pixel transfer curve for dark and illuminated states.

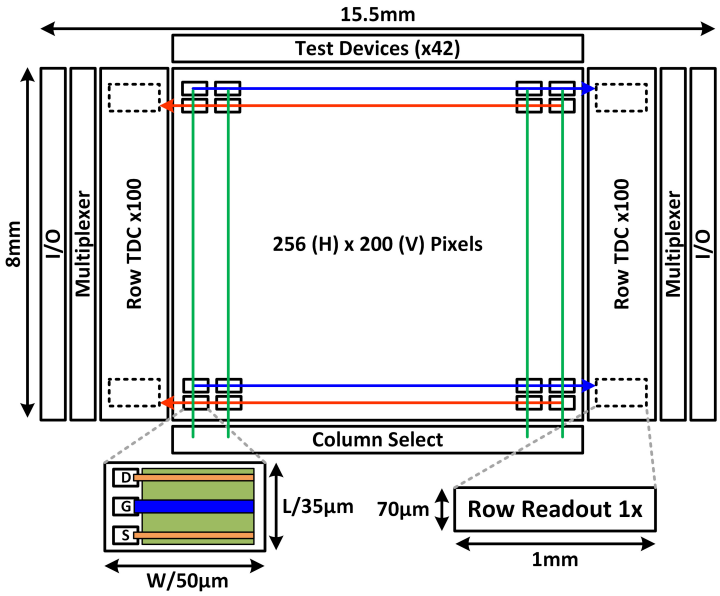

Figure 12.2.2: Chip Floorplan.

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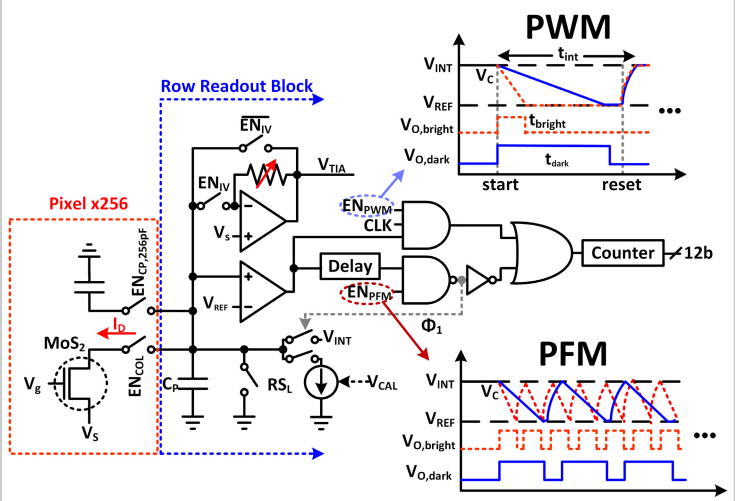

Figure 12.2.3: Device row schematic, showing connected column devices and readout circuits and waveforms for PWM and PFM measurement modes.

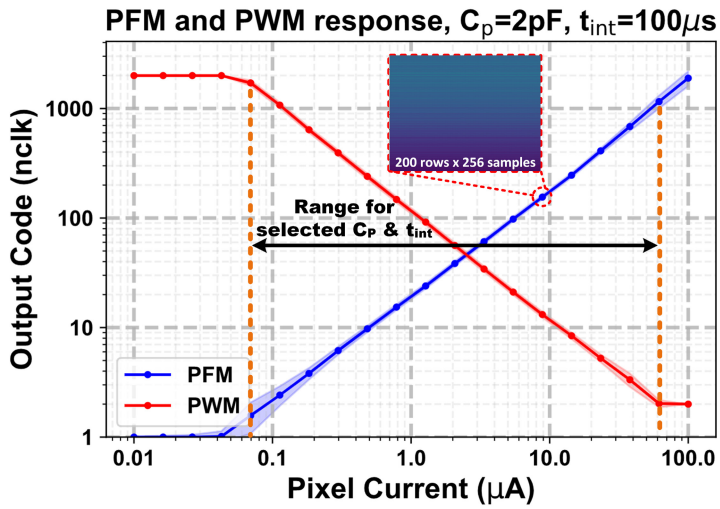

Figure 12.2.4: Readout circuit digital output for PWM and PFM operating modes during ID sweep from on-chip calibration circuit.

Figure 12.2.5: "Cameraman" Image Captured by 2D MoS2 Image Sensor.

	This work	[4] Nature Photonics '17	[3] Advanced Materials '20	[5] Nature Comms. '17
CMOS	0.18 µm	0.5 µm	No	No
ASIC	Yes	-	-	-
Array Size	256 x 200	388 x 288	32 x 32	12 x 12 (1)
Pixel Size	30 µm x 50 µm	35 µm x 35 µm	50 µm x 50 µm	300 µm x 300 µm
Material	MoS_2	Graphene Quantum Dot	MoS_2	MoS_2
Readout Integration	Yes (TDC)	Partial (Off-Chip ADC)	No	No
Pixel Terminals	3	2	3	3
On-Chip Resolution (bits)	12	-	-	-
Dynamic Range (dB)	76 (2)	55	-	-

(1) Effective imaging area

(2) Limited by pixel on/off ratio

Figure 12.2.6: Device Comparison Table.

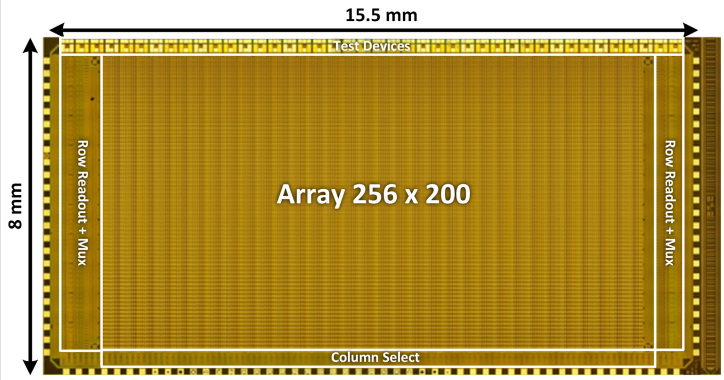

Figure 12.2.7: Chip micrograph.

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