Surpassing Tradeoffs by Separation: Examples in Frequency Generation Circuits

(*Invited Paper*)

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Abstract— **We review three examples (two PLLs [1], [2] and one on-chip transmission-line resonator [3]) of design tradeoffs which can in fact be circumvented; the key in each case is that the parameters that seem to trade off with each other are actually separated in time or space. This paper is an attempt to present these designs in such a way that this common approach can hopefully be applied to other circuits.**

Keywords— **Tradeoffs, transmission lines, oscillators, phase locked loops, frequency synthesizers, integrated circuits.**

I. Introduction

DEALING with tradeoffs is a challenge engineers must face in almost every design. A tradeoff occurs whenever one favorable parameter or performance measure must be sacrificed in favor of another. A classic example is the tradeoff between gain and bandwidth in amplifiers, usually constrained by a constant gain-bandwidth product. In the face of such a tradeoff one increases gain at the expense of bandwidth or vice versa until hopefully both values are acceptable. In this way tradeoffs often become the ultimate limitation upon the design.

However, sometimes it is easy to perceive a tradeoff where it can in fact be nullified: two parameters that seem to trade off with each other may actually be independent or separable with clever design.

To illustrate this point let us consider Crowley's widely-used phase-locked loop (PLL) [1] (**Example 1**), which turns out to be an example precisely of this nature. In this case the apparent tradeoff is that between lock time and spectral purity: on one hand, the loop bandwidth must be maximized to minimize lock time. On the other hand, too wide a bandwidth brings more spurs and component noise (except VCO noise) into the PLL's dynamics, corrupting its output spectrum. Due to their opposite dependencies on loop bandwidth, lock time and spectral purity appear to be conflicting traits. But these two traits actually have their significance in two separate phases of the PLL operation and are therefore separated in time: spectral purity matters only during steady-state and lock time matters only during transient. Recognizing the separability of these two traits in time, Crowley employs a variable bandwidth scheme: a wider bandwidth is used during transient to accelerate phase locking, but once the PLL enters a phase-locked steady state, the bandwidth is shifted to a smaller value to attain an optimal spectrum.

Two of our own recently published designs [2], [3] happen to follow the same design paradigm. Our PLL work by Woo *et al* [2] recognizes a separability in time between another set of PLL design parameters in an apparent tradeoff and exploits the separability in constructing a fastlock PLL. Our work by Andress *et al* [3] deals with a tradeoff between series and shunt losses in a microwave on-chip transmission line. While it is a common notion that reducing one type of loss without increasing the other is difficult, in [3] we show that if the amplitudes of waves hosted by the line are made position-dependent, as in a standing wave, the series and shunt losses can be separated in space and a high-Q transmission line can be built.

Though Crowley's work and our own two works are all based upon entirely different designs, we found in retrospect that they share the same spirit of circumventing certain tradeoffs through separation in time or space. Our objective in this paper is to illustrate this common observation, by reviewing our two works [2], [3] under this unified theme. Thus rather than introducing a new contribution we wish to explicitly articulate and share the insight common to these prior works, and we hope it can be related to other designs in the future. We will first discuss the work in [3] where the principle can be illustrated simply, and then move on to the work in [2] where the principle appears in a rather complicated fashion.

II. Example 2: Wave-Adaptive Tapered Transmission Line

In this section we consider an on-chip transmission line in silicon, and explore a tradeoff between two types of power dissipation in the line. The tradeoff can be circumvented by exploiting the spatial separation between the two losses whenever a standing wave is formed on the line. This work was originally published in [3].

For the on-chip transmission line, the focus will be specifically on a coplanar stripline (CPS) widely used for differential operation. It consists of two metals running in parallel. The CPS can directly face a silicon substrate underneath [Fig. 1(a)], or, floating metal strips periodically placed underneath the CPS [Fig. 1(b)] can shield fields from the lossy silicon substrate. In the latter case, the relatively large loss of the silicon substrate is replaced with the smaller loss of the floating metal strips.

A. Tradeoff between Series and Shunt Losses

The CPS structure can be electrically modeled using the familiar differential $LRCG$ network [Fig. 1(c)], where L, C,

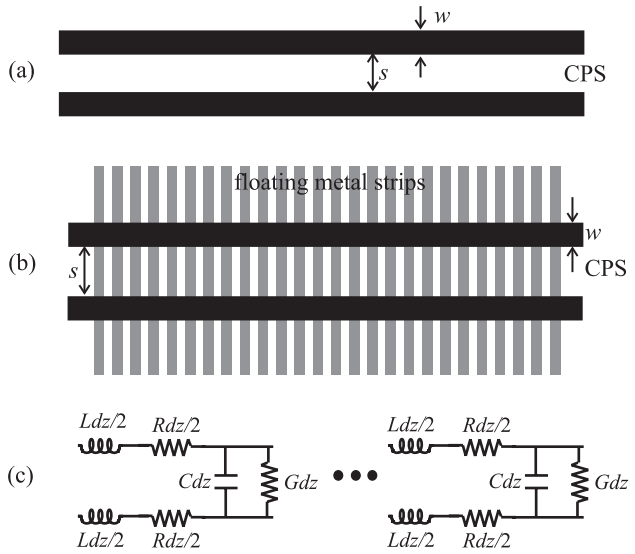

Fig. 1. (a) CPS above a silicon substrate (top view). (b) CPS with underlying metal strips above the substrate. (c) *LRCG* model.

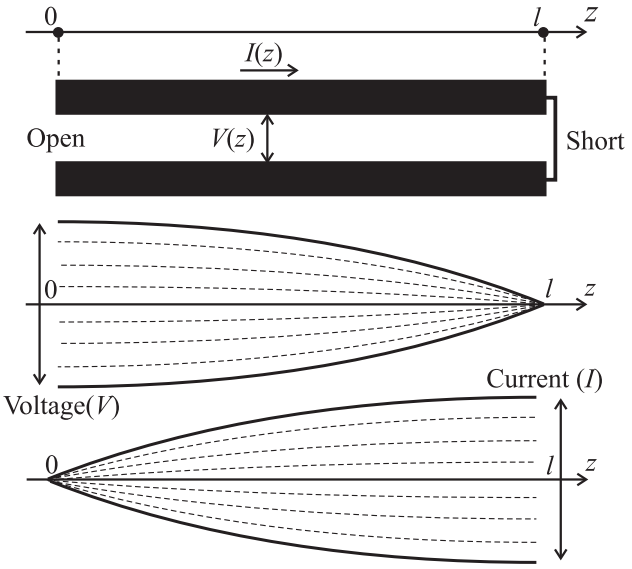

Fig. 2. A CPS with a short and an open termination at each end and the $\lambda/4$ voltage and current standing waves it hosts.

R, and G are inductance, capacitance, series resistance, and shut conductance per unit length, respectively. R mainly accounts for loss *within* the CPS metals due to skin and proximity effects. The familiar skin effect is the tendency for *ac* current to become concentrated at the surface of a conductor at high frequencies, thereby reducing the effective area of current flow. The proximity effect refers to the phenomenon that when two *ac* currents flow in opposite directions, the effective area of current flow is further squeezed toward the proximate regions of the two conductors. G, on the other hand, reflects loss *outside* of the CPS metals, for instance, losses coming from the substrate in the CPS of Fig. 1(a) and losses coming largely from the underlying periodic metal strips of Fig. 1(b).

R couples to current waves as G couples to voltage waves to introduce respective series and shunt losses. Smaller R corresponds to less series loss; smaller G corresponds to less shunt loss. Simultaneous minimization of R and G is desired in the design of the CPS by properly selecting its two design parameters, the metal width, w, and the separation, s, where w and s are with reference to Fig. 1. The simultaneous minimization, however, is difficult. Increasing w decreases R due to a reduced skin effect but increases G due to increased interaction between EM fields and lossy media outside the CPS metals (substrate or underlying metal strips). Likewise, increasing s mitigates proximity effects hence decreasing R, but this increases G again due to increased interaction between fields and lossy media outside the CPS metals. Clearly one cannot come up with a CPS structure where both R and G are simultaneously minimized. This is a widely recognized tradeoff between R and G, from which one might easily conclude that the series loss caused by R and the shunt loss caused by G cannot be simultaneously minimized.

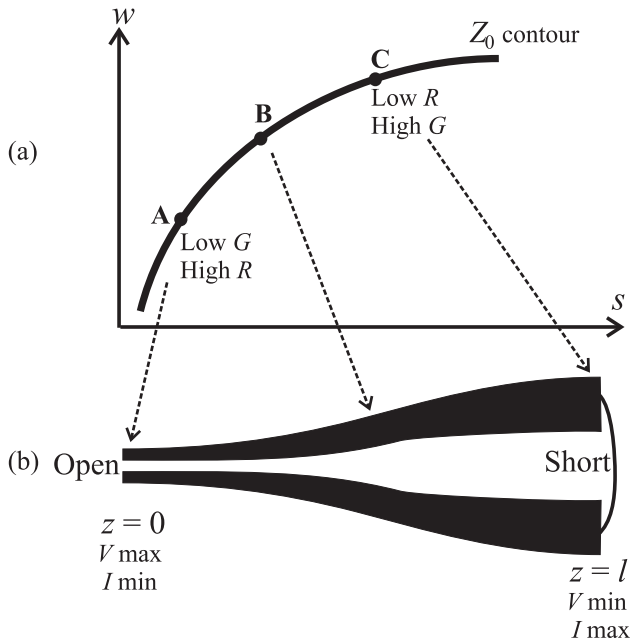

Fig. 3. (a) Z_0 contour in w-s space. (b) Tapered line.

B. Circumventing the Tradeoff via Line Tapering

A more careful inspection, however, reveals that such a conclusion is a hasty one. The series loss caused by R is also a function of the current wave amplitude, and the shunt loss caused by G is also a function of the voltage wave amplitude. If the line hosts a sinusoidal traveling wave where the voltage and current amplitudes are the same throughout the line, it is indeed true that the R-G tradeoff directly translates to the tradeoff between the series and shunt losses. However, if the CPS hosts a sinusoidal standing wave where the voltage and current amplitudes are position-dependent and moreover the voltage and current standing waveforms are offset from each other by a quarter wavelength in space, a completely different

scenario emerges and the R-G tradeoff can be elegantly circumvented so as not to cause the tradeoff between the series and shunt losses, in order to minimize overall loss [3].

To see this, consider a CPS of length l terminated by an open on one end and a short on the other, as in Fig. 2. Reflections of waves at both ends and their superpositions lead to standing waves. In the resulting fundamental standing-wave mode, the CPS would span a quarter wavelength ($l = \lambda/4$), with the voltage maximum & current zero at the open end ($z = 0$) and the current maximum & voltage zero at the short end ($z = l$): see Fig. 2. Since R couples to current waves, series losses are localized toward the short end ($z = l$). Likewise, since G couples to voltage waves, shunt losses are localized toward the open end ($z = 0$). In other words, the series loss and shunt loss are rather separated in space. When the two types of dissipation do not overlap significantly in space, the R-G tradeoff is quite irrelevant. Near $z = 0$, G may be minimized by choosing proper w and s to reduce loss while the unavoidable increase in R (due to the R-G tradeoff) is not detrimental because of the negligible current amplitude in this vicinity. Similarly toward $z = l$, R may be minimized to reduce loss while the inevitable increase in G is not harmful due to the locally negligible voltage. This continuous variation of R and G along z by varying w and s to minimize loss yields a tapered transmission line.

The CPS tapering while holding the characteristic impedance Z_0 constant throughout the line to prevent reflections can be done using a contour of characteristic impedance in w-s space obtained from EM simulations [Fig. 3(a)]. As one simultaneously moves apart (increasing s) and widens (increasing w) the CPS following this contour, Z_0 remains constant while R decreases and G increases (R-G tradeoff). The $\lambda/4$ CPS can be tapered along this contours as shown in Fig. 3(b). The voltage maximum and current zero at $z = 0$ yields minimum local loss with low G and high R. The current maximum and voltage minimum at $z = l$ yields minimum local loss with low R despite high G. In [3] we experimentally confirmed the benefit of this technique: a lower-loss (higher-Q) tapered structure, when used as a resonator of a standing wave oscillator, lowers the oscillator's phase noise by 10 dB.

The separability between lock time and optimum spectrum in two distinct phases of the PLL operation lends itself to Crowley's technique of varying the PLL bandwidth in time. Analogously, the separability between the series and shunt losses in two distinct points of a transmission line hosting a standing wave lends itself to our technique of varying the line structure in space.

III. Example 3: PLL Frequency Synthesizer Combining Fractional- & Integer-N Modes

Crowley's fast-lock variable-bandwidth PLL [1] has been used almost exclusively within a fixed frequency division mode, *i.e.*, the bandwidth switching has been executed while maintaining the same frequency division mode at either integer- or fractional-N. In [2], we generalized Crowley's scheme, introducing a single-loop fast-lock PLL frequency synthesizer that changes not only bandwidth but also frequency division mode between transient and steady states. More concretely, the PLL operates in a narrow-bandwidth, integer-N mode during steady state (phase lock), but in a wide-bandwidth, fractional-N mode (with no fractional spur reduction circuit such as phase interpolators or high-order $\Sigma\Delta$ modulators) during transient. See Fig. 4. This hybrid PLL frequency synthesizer is another example in which an apparent tradeoff is circumvented via separation in time, which we will elucidate in what follows.

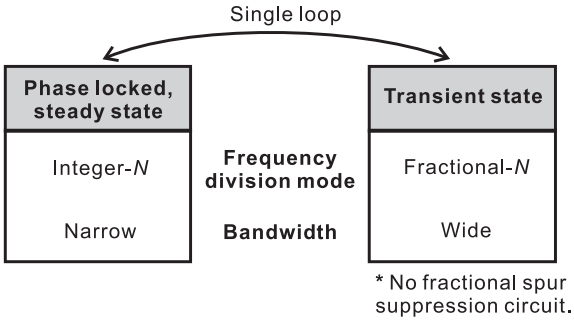

Fig. 4. Hybrid PLL operation.

A. Tradeoff & its Circumvention

Consider a scenario where an integer-N PLL frequency synthesizer is preferred to a fractional-N one, due to the design simplicity of the former. In the latter, phase interpolators or high-order $\Sigma\Delta$ modulators are needed to reduce fractional spurs. Since quantization noise of such fractional spur reduction circuits can corrupt the PLL spectrum via loop nonlinearities, significant design efforts are required to minimize loop nonlinearities in the fractional-N PLL. In contrast, integer-N PLLs are much simpler to design due to the absence of fractional spurs.

The design simplicity of integer-N PLLs, however, comes at the price of slow locking. To produce the same set of output frequencies in a given application, an integer-N PLL uses a lower reference frequency than a fractional-N PLL. The reference frequency is directly proportional to the maximum usable bandwidth in any PLL, and hence, the integer-N PLL cannot accommodate as large a bandwidth as the fractional-N PLL. The result is the slower speed of the integer-N PLL.

So an apparent tradeoff would be encountered in an attempt to achieve both the speed of the fractional-N PLL and design simplicity of the integer-N PLL. In [2] we recognized, however, that the two traits involved in the tradeoff, speed and fractional spurs (the latter is tied with the design complexity as mentioned), matter in two separate phases of the PLL operation, the exploitation of which led to the hybrid PLL. During transient, the speed is what matters and hence we use a fractional-N mode that can accommodate a larger bandwidth. During steady state, the PLL is shifted to integer-N since the continued use of the fractional-N in the steady state would require the fractional-spur reduction circuit. The use of the fractional-N mode only during transient does not require such a fractional spur re-

duction circuit, for spurs matter only during steady state, and hence we do not implement any such fractional spur reduction circuit, leading to the design simplicity. In this way we came up with the hybrid PLL that opportunistically switches between the two frequency division modes of differing bandwidths to circumvent the apparent tradeoff, adopting each of their good behaviors while discarding their bad behaviors.

The hybrid PLL may be viewed as an integer-N PLL made faster than the normal integer-N PLL by borrowing the speed of the fractional-N PLL during transient. Integer-N PLLs have inherently worse phase noise than fractional-N PLLs. Therefore, in a situation where the phase noise is to be made as small as possible, the hybrid PLL would not be an optimal design choice (as phase noise is a concern in steady state) and the aforementioned tradeoff would not enter the design considerations. However, when an integer-N PLL can meet target phase noise specifications in certain applications (GSM, Bluetooth, and WLAN, for instance) [2], the hybrid PLL can be a valuable design choice.

The hybrid PLL example has again illustrated how an apparent tradeoff can be surpassed via separation. Although the main point of this paper has now been delivered, below we will briefly describe the hybrid PLL's architecture and operation for the sake of completeness.

B. Architecture & Operation

Fig. 5 shows the architecture of the hybrid PLL. When the PLL enters a transient state, the two static divide-by-M blocks are disabled and screened out by the two multiplexers, and the crystal oscillator signal $x(t)$ [frequency: f_0] and the prescaler output, $d_1(t)$, are fed to the PFD. This is a standard fractional-N PLL configuration but with no fractional spur reduction circuit. The standard prescaler-accumulator combination inside the dashed box provides a fractional division ratio of $N_d = N + k/M$ through $d_1(t)$. The reference frequency is f_0.

When the PLL attains a phase lock, both divide-by-M blocks are enabled and their outputs, $x_1(t)$ and $d_2(t)$, are fed to the PFD through the two multiplexers. This reconfigured loop is an integer-N PLL: the reference frequency is f_0/M; the integer frequency division ratio of $N_d = NM+k$ is provided through $d_2(t)$ by the rather unfamiliar combination of the accumulator, divide-by-M, and prescaler inside the dashed box. The resulting set of output frequencies are the same as in the fractional-N mode.

The simple switching between the two modes is enabled by the absence of fractional spur reduction circuits, and that the overall hybrid PLL of Fig. 5 is almost the normal integer-N PLL, with only 3 additional, simple digital components (shaded areas).

Execution of the mode switching in sync with bandwidth switching is at the heart of the hybrid PLL operation.

In conventional Crowley's variable-bandwidth PLLs, the charge pump current I_0 and the loop filter resistance R are changed together to shift the loop bandwidth while maintaining the same phase margin in the loop gain transfer

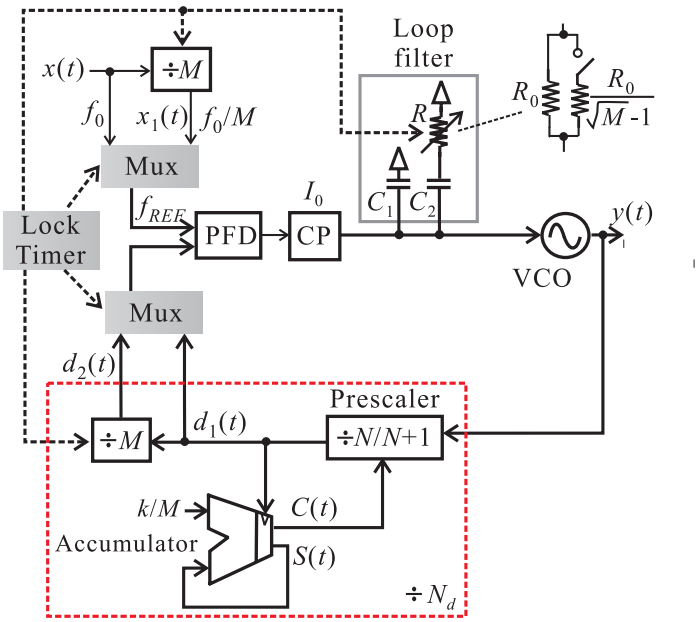

Fig. 5. Overall architecture of the hybrid PLL frequency synthesizer

function [1]. In our hybrid PLL, the frequency division ratio N_d naturally changes upon bandwidth switching due to the simultaneous mode switching, and this can serve as an additional parameter in altering the loop bandwidth. This feature permits exploration of a larger design space for bandwidth switching, *e.g.*, when the bandwidth is to be changed by a large amount, this new protocol can lessen the burden of the large I_0-change, as the N_d-change can also contribute. An especially interesting scheme is to not change I_0 at all, but to solely rely on the change of N_d for altering the loop bandwidth (R has to be always changed). This represents a more digital fashion of bandwidth switching, a polar opposite of the conventional bandwidth shifting where I_0 must be altered.

Our experimental work in [2] firmly confirms the benefit of our hybrid PLL. There are many implementation details, for which we can refer the readers to [2].

IV. Conclusion

We have discussed several published design examples in which tradeoffs can be surpassed if the relevant traits are somehow separated in time or space. We hope that the perspective presented in this paper can be applied to other designs.

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