9.3 All-Digital Dynamic Self-Detection and Self-Compensation of Static Phase Offsets in Charge-Pump PLLs

Yong Liu[1], Woogeun Rhee[2], Daniel Friedman[2], Donhee Ham[1]

[1]Harvard University, Cambridge, MA
[2]IBM T.J. Watson, Yorktown Heights, NY

The widely-used IC design paradigm of dynamic self-compensation for on-chip variability [1] proved also fruitful in the design of charge-pump phase-locked loops (CP-PLLs). In [2,3], auxiliary feedback loops were added to CP-PLLs in order to detect and correct static phase offsets caused by on-chip variability. Such dynamic self-compensation in CP-PLLs is useful because static phase offsets can cause problems in CP-PLL applications, notably, clock alignment in data links and microprocessors. All-digital approaches can be especially attractive with continuing device scaling.

We report a CP-PLL incorporating an all-digital auxiliary feedback loop that detects static phase offsets and adjusts them down to a value less than a preset, target offset. While all-digital auxiliary feedback loops to compensate for static phase offsets *per se* are not new (*e.g.*, [2,3]), the operation with the preset, target static phase offset distinguishes this work. This approach makes possible a quantitative on-chip monitoring of the static phase offset, leading to its reliable compensation without blind operation. This on-chip monitoring may also be incorporated in on-site manufacturing verification processes for on-chip variability.

The CP-PLL is shown in Fig. 9.3.1. The lower portion is a standard CP-PLL, while the upper portion is the all-digital static phase offset compensation loop. The compensation loop consists of three blocks: the instantaneous phase error detector (Box 1), the unit that extracts static phase offset information from the instantaneous phase error (Box 2), and the unit (Box 3) that produces a digital control code to adjust charge-pump currents based on the static phase offset information produced by Box 2.

The operation of the instantaneous phase error detector (Box 1, Fig. 9.3.1) can be understood in connection with Fig. 9.3.2. The purpose of PFD1 is to replicate the instantaneous phase error of interest, ΔT, between the reference signal, *REF*, and divider output signal, *DIV*, into the instantaneous phase difference between the rising edges of signals *A* and *B*, and at the same time, to align the falling edges of *A* and *B* for subsequent processing. The logic circuit of the instantaneous phase error detector (Box 1) processes *A* and *B* to provide information on the magnitude and polarity of ΔT in output signals *M* and *P*. *M* indicates whether ΔT is larger or not than T_{win}, where T_{win} is a target static phase offset. This T_{win} is preset in a chain of current-starved inverters by tuning bias currents, where the chain is shown as a delay element in Fig. 9.3.1. If $\Delta T > T_{win}$, $M = 1$ (Fig. 9.3.2, left and middle). Otherwise, $M = 0$ (Fig. 9.3.2, right). On the other hand, *P* is an output of a bang-bang phase detector (DFF1, Fig. 9.3.1), and indicates the polarity of ΔT: if *B* leads *A* (Fig. 9.3.2, left), $P = 0$; otherwise, $P = 1$ (Fig. 9.3.2, middle).

To extract static phase offset information from *M*, an accumulator-based digital averaging circuit (Box 2, Fig. 9.3.1) measures *M* over 64 reference clock periods, and outputs 1 at *M'* if *M* has a greater number of 1's than 0's, and otherwise outputs 0 at *M'*. *M'* therefore indicates whether the magnitude of the *static* phase offset is smaller than T_{win}. This process is needed to average out jitter effects in instantaneous phase errors and high-frequency variations in T_{win}. The digital control logic (Box 3, Fig. 9.3.1) processes *M'* and *P* to produce a digital control code. The control code adjusts charge-pump currents to compensate for the static phase offset. The polarity signal, *P*, adjusts the charge-pump currents step by step until the static phase offset becomes smaller than T_{win}, i.e., until *M'* becomes zero. *M'* is monitored to start and end the compensation process.

In addition to signals *M* and *P*, the instantaneous phase error detector (Box 1, Fig. 9.3.1) produces signal *L*. This is obtained exactly the same way as *M*, but using a preset time, T_{lock}, which is much larger than T_{win}. *L* is used to indicate an onset of phase lock. Once *L* signals lock detection, the static phase offset compensation process is started.

The charge pump with digitally controllable auxiliary current sources is shown in Fig. 9.3.3. The digital control codes, C_{UP}<4:0> and C_{DN}<4:0>, arriving from the digital control unit (Box 3, Fig. 9.3.1) adjust auxiliary current sources, I_{C1} and I_{C2}, to reduce the static phase offset. The total current adjustment range is ±32% of the main charge-pump current I_0. During compensation, I_{C1} or I_{C2} changes for every step by 0.5% of I_0. Such a small current change guarantees that the PLL remains locked throughout the compensation process. The time required to complete the compensation is proportional to the initial static phase offset and is typically a few milliseconds. This time is long enough so that the compensation does not materially interfere with the PLL's own loop dynamics, yet short enough to correct the static phase offset variation caused by, for example, low-frequency deviations of supply and temperature.

The CP-PLL architecture of Fig. 9.3.1 is implemented in 90nm 1.2V CMOS to verify the proposed compensation scheme for a clock generation application. The design clock and reference frequencies are 6GHz and 300MHz, respectively. The compensation loop occupies 7% of the total active area and consumes 0.3% of the total 16mW power dissipation. The chip core of Fig. 9.3.4 shows a layout because functional blocks are covered by metal fills in the micrograph.

In experiments, the target offset, T_{win}, is calibrated off chip and the minimum achievable T_{win} is 15ps. This value is limited by delay mismatches in the layout and could be reduced with an improved physical design of the relevant critical paths. In real manufacturing, T_{win} can be on-chip calibrated using a standard ring oscillator method, also taking into account the long-term variation of T_{win}.

The top of Fig. 9.3.5 shows the measured static phase offset as a function of the VCO control voltage with and without the compensation scheme. The VCO control voltage, V_C, is used to intentionally introduce static phase offset (due to finite output impedance of current sources, variations in the VCO control voltage cause charge-pump current mismatch) to verify the functionality of the compensation loop. As V_C is swept, the static phase offset change is 600ps (18% of the reference period, 3.33ns) with the compensation loop disabled. With the loop enabled, however, the static phase offset is always kept within ±15ps (T_{win}) and the compensation control code is linearly proportional to the initial static phase offset, clearly demonstrating the effectiveness of the compensation loop.

Although this approach is aimed at minimizing static phase offsets and is not necessarily optimal in reducing reference spurs, the latter is correlated to the former and hence, we measure reference spur reduction resulting from the compensation to further verify the proposed scheme. The bottom of Fig. 9.3.5 shows measured spurs at various VCO control voltages with and without compensation. Each data set for a given control voltage is obtained from measured power spectra (Fig. 9.3.6 is an example). The spurs are always smaller when the compensation is enabled.

To further verify the compensation scheme, yet another measurement is made (Fig. 9.3.7). By changing the supply voltage, a varying degree of static phase offsets is introduced. A larger offset requires an increased number of correction steps, providing another clear evidence of the workings of the compensation loop. This also shows that this scheme is suitable to compensate for static phase offsets arising from low-frequency supply variations.

Acknowledgements:
We thank B. Parker, A. Chung, and K. Jenkins of IBM and K. Woo and G. Wei of Harvard.

References:
[1] H.-S. Lee, D.A. Hodges, and P.A. Gray, "A Self-Calibrating 15 Bit CMOS A/D Converter," *IEEE J. Solid-State Circuits*, vol. 19, no. 6, pp. 813-819, Dec., 1984.
[2] G. Wei, J.T. Stonick, D. Weinlader, et al., "A 500MHz MP/DLL Clock Generator for 5Gb/s Backplane Transceiver in 0.25µm CMOS," *ISSCC Dig. Tech. Papers,* pp. 464-465, Feb., 2003.
[3] A. Tan and G. Wei, "Phase Mismatch Detection and Compensation for PLL/DLL Based Multi-Phase Clock Generator," *IEEE CICC*, pp. 417-420, Sep., 2006.

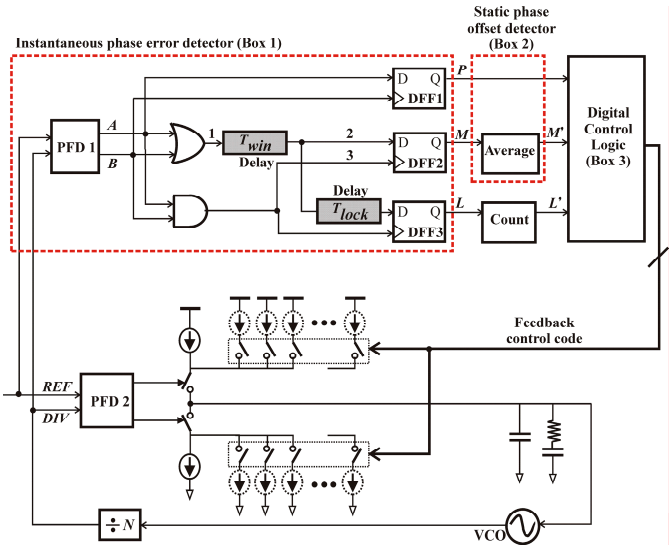


Figure 9.3.1: The proposed charge-pump PLL with the static phase offset compensation.

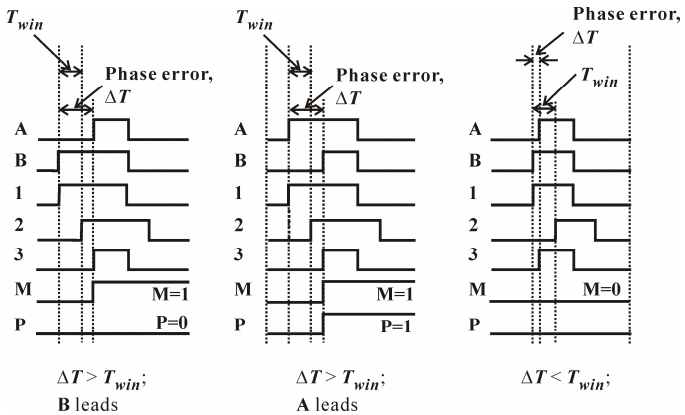


Figure 9.3.2: Timing diagram of the instantaneous phase offset detector (Box 1, Fig. 9.3.1).

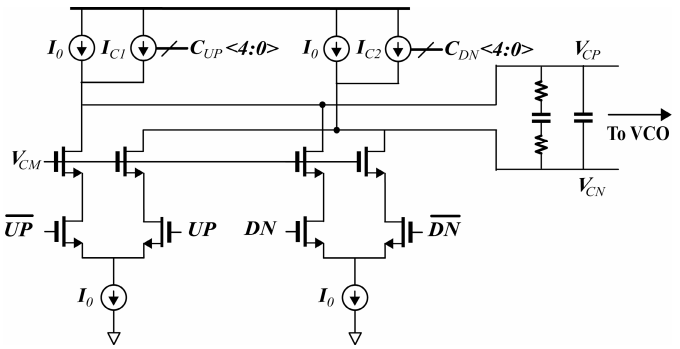


Figure 9.3.3: Charge pump with auxiliary current sources.

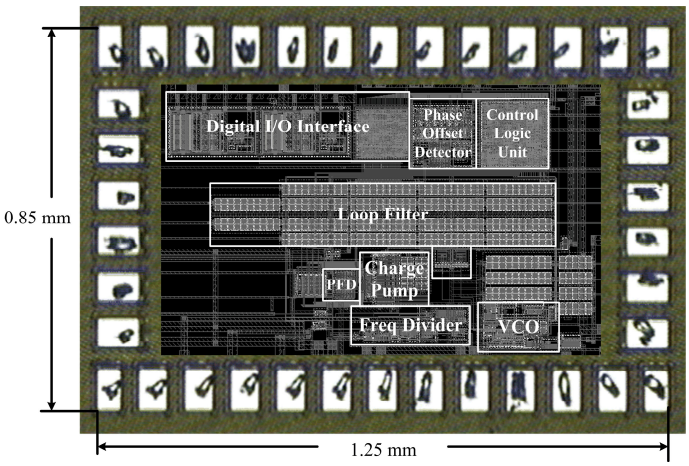


Figure 9.3.4: Chip micrograph (with layout for the chip core).

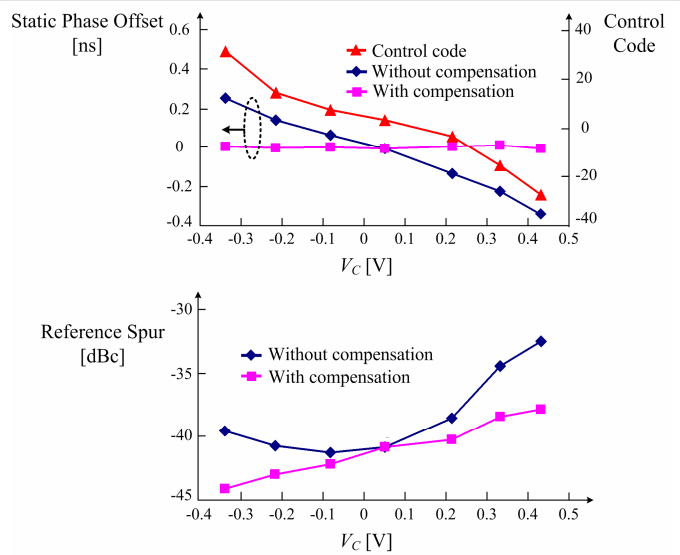
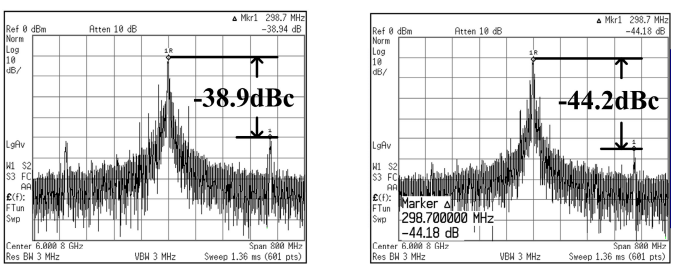


Figure 9.3.5: Measured static phase offset compensation and reference spur reduction.



Without Compensation | With Compensation

Figure 9.3.6: Measured clock spectrum.

Continued on Page 595

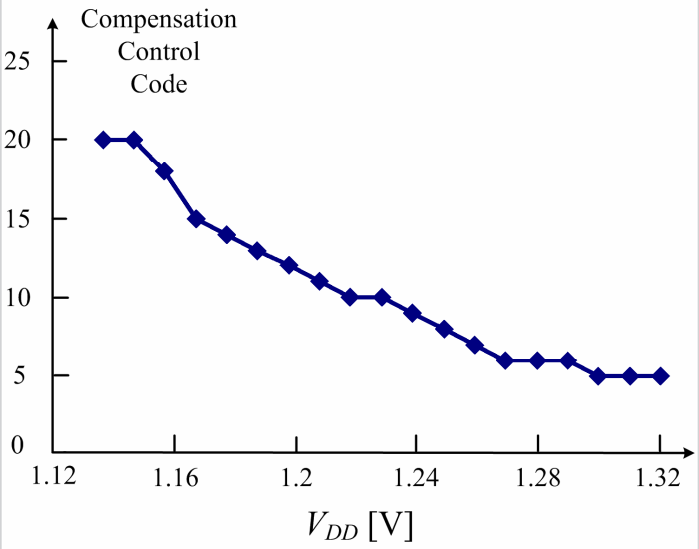


Figure 9.3.7: Measured compensation control code when power supply varies.

