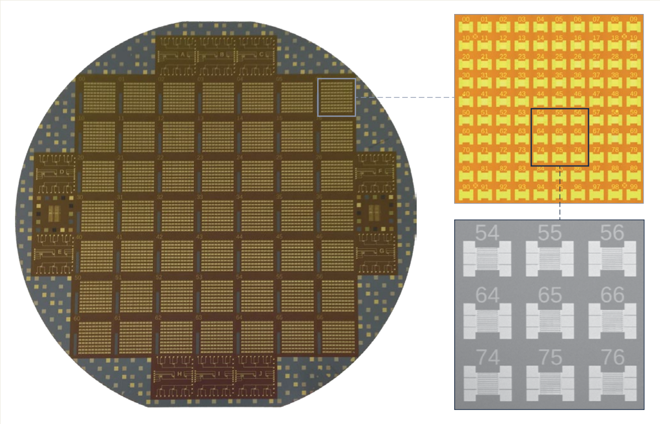
https://doi.org/10.1038/s41566-022-01093-w

Optoelectronics

# Computing with silicon photodiodes

In standard CMOS image sensors, image acquisition and processing are separate tasks that take place in different locations. Typically, a front-end silicon photodiode array converts the incident light into analogue electric currents, while an electronic back-end digitizes the currents for further processing. However, this approach brings increased memory usage, power consumption and latency. Now, writing in *Nature Electronics*, Jang and colleagues demonstrate an alternative solution: silicon photodiode arrays that simultaneously capture and process images in a CMOS-compatible platform (*Nat. Electron.* **5**, 519–525; 2022).

Key to this success is the use of electrochemically doped silicon photodiodes, as opposed to traditional electrostatically doped devices. By fabricating metallic contacts on intrinsic silicon, a bias voltage produces localized and electrically programmable p–i–n or n–i–p regions. Modification of the gate voltage modulates the responsivity $R$ of the photodiode. Upon exposure to light with power $P$, a photodiode effectively performs a multiplication, where the photocurrent $I$ is obtained as $I = R \times P$.



When currents generated by all photodiodes in an array are summed, the array effectively performs a multiply–accumulate operation. By spatially programming the responsivity on a pixel-by-pixel basis, the array can serve as an image filter kernel for convolutional image computation. The spatial programming ability is challenging to achieve with traditional electrostatically doped substrates, where the responsivity is fixed, as determined by the doping density of the silicon wafer.

The authors first show the suitability of the approach to wafer-level fabrication by realizing arrays of almost 5,000 photodiodes (see image). By testing a subset of 3,500 photodiodes, 94% of them could be successfully programmed electrically. As a demonstration of the simultaneous imaging and computing ability, the authors employ a smaller 3 × 3 network of connected photodiodes to detect the movement of a laser spot. The spatial distribution of the programmed responsivities over the 9 pixels acts as a computing kernel to perform edge detection via the change of polarity of the summed photocurrents as the laser spot is swept over the network.

The team then go on to demonstrate the capture and image processing of a 256 × 256 image. Patches of the image are projected onto the photodiode array by using light spots from an LCD projector. As the entire image is projected sequentially in 3 × 3 patches, the resulting convolution operation produces images processed with image filters such as a Sobel filter, a Gaussian blur or a sharpening filter, as determined by various image filtering kernels programmed into the photodiode array.

The present demonstration is still relatively small-scale and integration with CMOS foundry-level processes still needs to be pursued, with the complexity of the interconnections between individual sensors to be carefully considered. In the future, scaling up the size of the array from 3 × 3 to larger networks will make it possible to capture an entire scene at once and create the opportunity to implement multiple filter kernels across the array. While challenges remain, this proof-of-principle demonstration represents an important step forward that indicates that in-sensor computing is feasible and compatible with CMOS architectures, and potentially able to deliver image filtering performance comparable to standard digital back-end processing designs.

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