

A Cyto-Silicon Hybrid System with On-Chip Closed-Loop Modulation

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Abstract—We introduce a bioelectronic interface between biological electrogenic cells and a mixed-signal CMOS integrated circuit with an array of surface electrodes, where not only is the CMOS electrode array capable of electrophysiological recording and stimulation of the cells with 1,024 recording and stimulation channels, but it can also provide low-latency artificial signal pathways from cells it records to cells it stimulates. This on-chip closed-loop modulation has an intrinsic latency less than 5 μ s. To demonstrate the utility of the on-chip closed loop modulation as an artificial feedback pathway between biological cells, we develop a silicon-cardiomyocyte self-sustained oscillator with a tunable frequency to which both the relevant part of the CMOS chip and cells are locked, and also a silicon-neuron interface with a silicon inhibitory connection between neuronal cells. This line of cyto-silicon hybrid system, where the boundary between biological and semiconductor systems is blurred, may find applications in prosthesis, brain-machine interface, and fundamental biology research.

Index Terms—CMOS integrated circuit, electrode array, electrophysiology, neurons, cardiomyocytes, bioelectronics, intracellular recording, extracellular recording.

I. INTRODUCTION

SILICON (CMOS) integrated circuit (IC) chips with surface electrode arrays interfaced with electrogenic cells—such as neurons and cardiomyocytes—can record the cells’ electrophysiological signals and can also manipulate, via stimulation, their electrophysiological behaviors [1], [2], [3], [4], [5]. One pursuit for these bioelectronic interfaces is to use the silicon chip to artificially substitute or augment biological functions for prosthesis and brain-machine interface, as well as for fundamental biology research [6], [7], [8], [9], [10], [11], [12], [13], [14]. Central to this pursuit is the

Received 23 June 2024; revised 21 August 2024; accepted 13 September 2024. Date of publication 23 September 2024; date of current version 29 May 2025. This work was supported in part by the Samsung Advanced Institute of Technology (SAIT) under Grant A37734 and in part by the Army Research Office under Grant W911NF-17-1-0425. This paper was recommended by Associate Editor X. Liu. (Jun Wang, Seok Joo Kim, and Wenxuan Wu contributed equally to this work.) (Corresponding author: Donhee Ham.)

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Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TBCAS.2024.3466549>.

Digital Object Identifier 10.1109/TBCAS.2024.3466549

ability to perform closed-loop (feedback) modulation, *i.e.*, recording signals from cells from a cellular network and providing appropriate stimulations back to cells in the same network, based on the signals recorded. Such closed-loop modulation was pioneered by earlier works [1], [7], [15], [16], [17] [18], yet there remains a room for significant improvement. For example, Refs. [1], [7], and [17] used off-chip processing in closed-loop modulation, which increases the latency between recording and stimulation. Taking another example, while Refs. [15], [16], and [18] used on-chip closed-loop modulation, they had a limited number of recording and stimulation channels (with the maxima for recording and stimulation being 64 [16] and 256 [18]), which limits the information that can be acquired by the recording and restricts the degree of manipulation.

Here we make improvement by developing a CMOS IC with a surface electrode array, which is capable of on-chip closed-loop modulation with 1,024 channels for both recording and stimulation [Fig. 1]. Concretely, the CMOS electrode array features $32 \times 32 = 1,024$ surface electrodes, each of which is connected to its own analog front-end (AFE) unit in the CMOS chip. This AFE unit can record cells and detect action potentials (APs), *a.k.a.*, spikes, with a voltage amplifier and a spike detector, and can stimulate cells with a current injector. Therefore, each pair of an electrode and an AFE unit, which we call a ‘pixel’, can serve as either a recording channel or a stimulation channel. Importantly, the CMOS IC also has global digital event processors (EPs), which supervise on-chip closed-loop modulation between any arbitrary recording and stimulation channels. The on-chip closed-loop modulation combined with the increased number of recording/stimulation channels is the chief advance this work represents. In addition, our CMOS electrode array can perform not only the usual extracellular recording but also intracellular recording, contrasting earlier closed-loop modulation works [1], [7], [15], [16], [17], [18] that relied on extracellular recording only. The intracellular recording is sensitive, and also enables a single electrode to access a single cell [2].

To demonstrate the operation of our CMOS electrode array with closed-loop modulation, we culture rat cardiomyocytes *in vitro* on the CMOS chip and operate this silicon-cardiomyocyte hybrid system as a self-sustained oscillator, whose frequency is tuned by the CMOS chip. Similarly, we develop a silicon-neuron hybrid system with rat neurons cultured *in vitro* on the CMOS chip, where the chip offers an artificial inhibitory connection between neurons. These silicon-cell hybrid systems blur the boundary between biological and semiconductor subsystems.

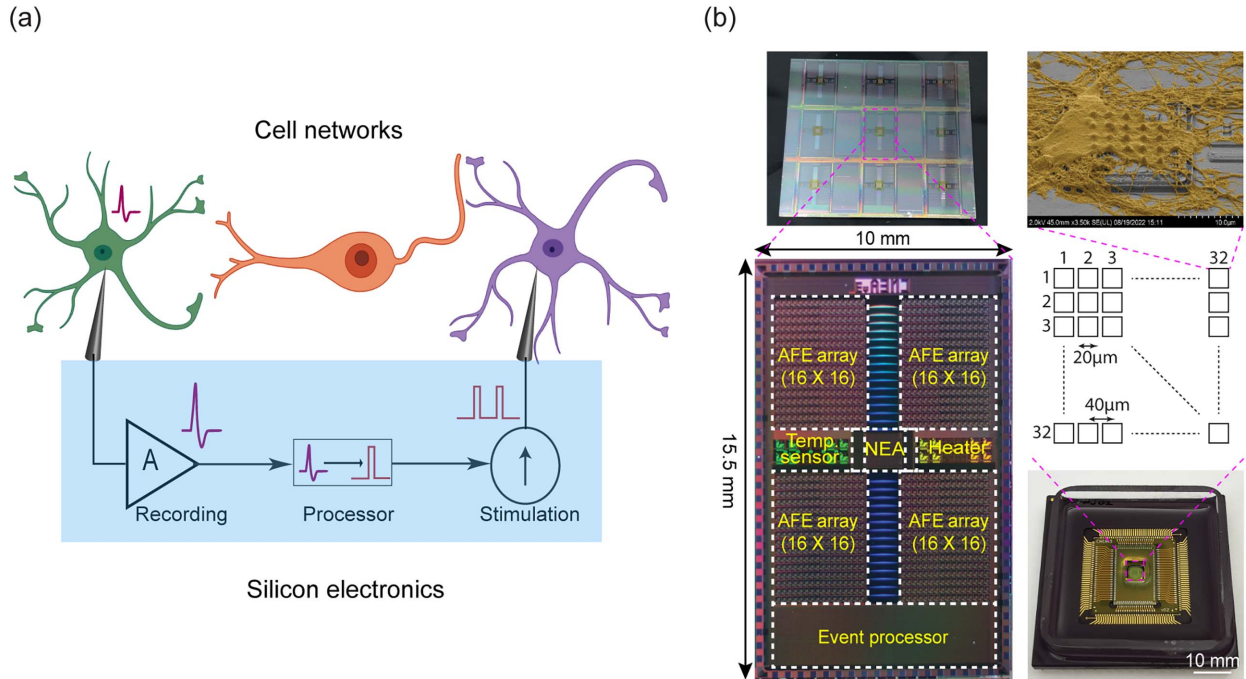


Fig. 1. (a) Illustration of on-chip closed-loop modulation with our CMOS electrode array. (b) (Left) micrograph of the CMOS IC. (Top right) SEM image of the CMOS electrode array with neurons cultured on top. Actual electrophysiological experiments are done with much higher population densities of neurons. (Middle right) dimensions associated with the 32×32 electrodes. (Bottom right) packaged chip.

The present paper is an extension of our prior conference paper [19]. Section II presents the architecture of the CMOS IC. Section III details the design and characterization of the main building blocks of the CMOS IC. Section IV describes the development of the CMOS electrode array from the CMOS IC chip via post fabrication, experimental setup, and electrophysiological recording with the CMOS electrode array. Section V presents closed-loop modulation experiments with cardiomyocytes and neurons.

II. ARCHITECTURE OF THE CMOS IC

The CMOS IC comprises an array of $32 \times 32 = 1,024$ surface electrodes at its center, a corresponding array of 1,024 AFE units at its four quadrants, and 10 globally shared digital EPs [Figs. 1(b) and 2]. As mentioned earlier, we call an electrode and an AFE unit connected to it together as a pixel. Each AFE unit contains recording, detection, and stimulation blocks (RB, DB, and SB). An electrophysiological signal from a cell or cells coupled to an electrode of a pixel is amplified by the pixel's RB, and then processed by the spike detector in the pixel's DB, which converts each detected spike into a digital pulse and sends it to an EP. The EP, in turn, issues a configuration signal to a destination pixel. The SB of this destination pixel then injects a stimulation current to its own electrode, where the timing and duration of the current injection is informed by the configuration signal from the EP. This completes the closed-loop modulation pathway.

While we have described a closed loop connecting a single recording pixel and a single destination (stimulation) pixel via a single EP for brevity, any single recording or destination

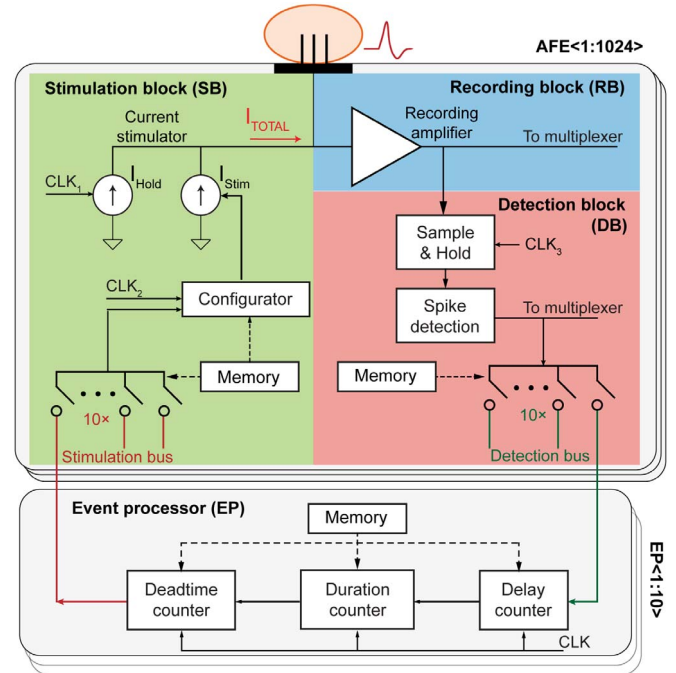


Fig. 2. Architecture of the CMOS IC, which contains 10 global EPs and an array of 1,024 AFEs.

pixel can be connected to up to 10 EPs concurrently, and each EP can receive inputs from any of 1,024 pixels simultaneously and issue configuration signals to any of 1,024 pixels simultaneously. The chip also integrates a heater and a temperature sensor [Fig. 1(b)] to help maintain the optimal environment for the cell culture.

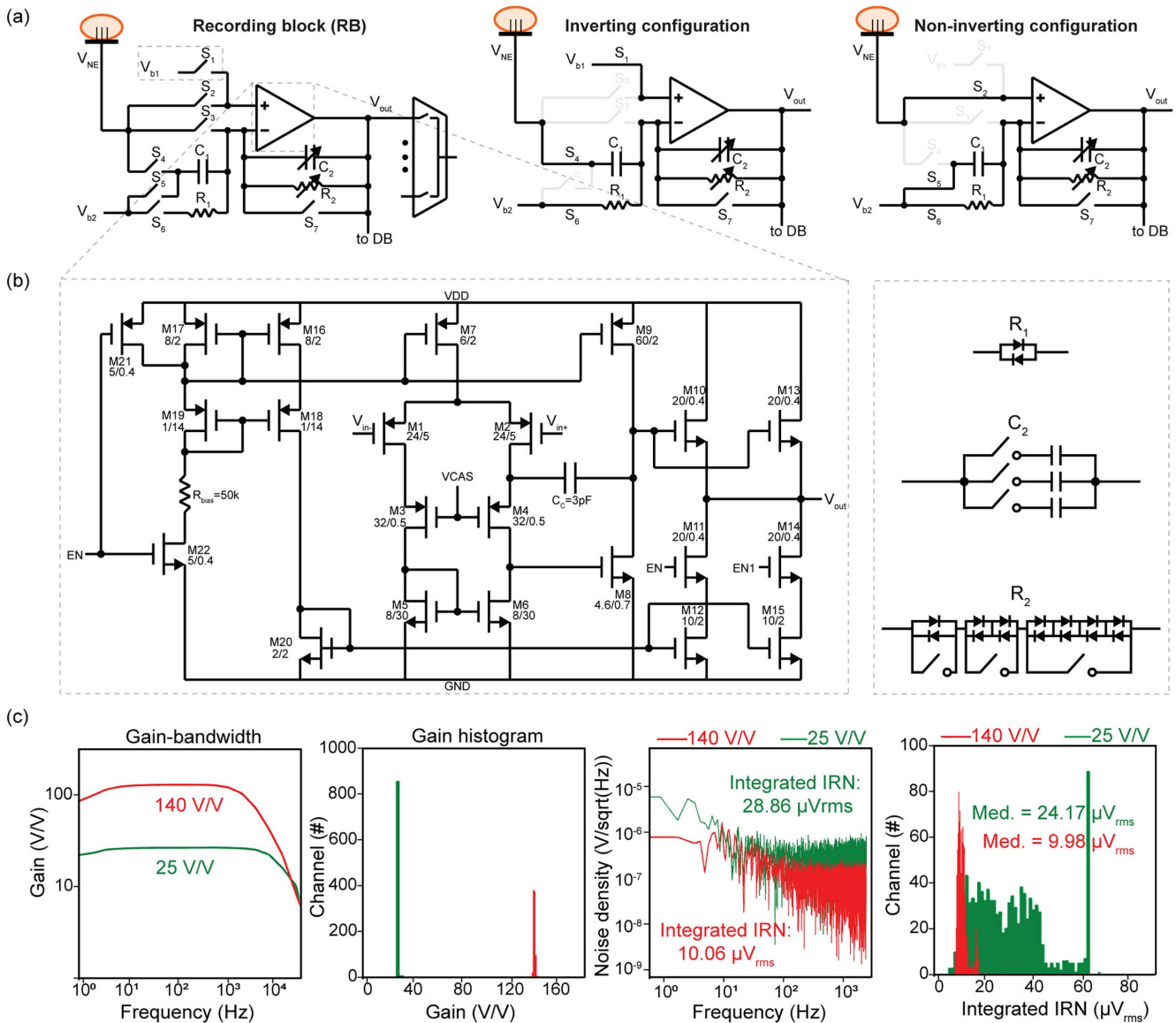


Fig. 3. (a) RB amplifier and its inverting and non-inverting configurations. (b) Transistor-level schematic of the op-amp (left), and schematics of R_1 , C_2 , and R_2 (right). (c) From left to right, measured gain magnitude vs. frequency of an RB inverting amplifier, histogram of measured flat band (sampled at 500 Hz) gain magnitudes of all 1,024 RB inverting amplifiers, measured IRN power spectral density vs. frequency of an RB inverting amplifier, and histogram of measured integrated IRN (integration bandwidth: 0.5 Hz–5 kHz) of the 1,024 RB amplifiers are shown for both intracellular (green) and extracellular (red) scenarios.

III. DESIGN AND CHARACTERIZATION OF THE CMOS IC

Here we describe the design and characterization of each key functional building block of the CMOS IC (the measurement setup itself is described in Sec. IV-B). Target performance specifications for these building blocks are to enable electrophysiological work, as we will detail in what follows.

A. Recording Block (RB)

Fig. 3(a), left, illustrates the schematic of the RB, which is an op-amp [Fig. 3(b)] with a negative feedback. This RB amplifier can be configured into a variety of operating modes by exploiting the 7 transmission gate switches (S_1, S_2, \dots, S_7), e.g., inverting and non-inverting modes of Fig. 3(a), middle and right. The non-inverting mode was designed to record both the AC and DC

parts of the electrophysiological signal, but we later realized that the recorded DC level reflects not only the electrophysiological effects but also the electrode offsets, and hence, in this work, we operate the RB amplifier in the inverting mode, which is an AC-coupled bandpass amplifier. Throughout this paper, however, all the recording traces presented are referred back to the input terminal of the amplifier, or the V_{NE} node (electrode node) of Fig. 3(a), middle, and thus voltage inversion is not shown explicitly.

The magnitude of the voltage gain of the inverting amplifier [Fig. 3(a), middle], C_1/C_2 , is made tunable by making C_2 adjustable (C_1 is fixed at 3.5 pF). To this end, C_2 is built with three metal-insulator-metal capacitors (4.6 fF, 21 fF, and 103 fF) and three switches [Fig. 3(b), right] and switch on-off combinations tune C_2 and thus the amplifier gain C_1/C_2 (in reality, due to the

parasitic capacitance, approximately 20 fF to 35 fF, in the feedback path of the amplifier, the gain magnitude somewhat differs from C_1/C_2 . The typical gain used is 25 for intracellular recording and 140 for extracellular recording. This gain difference is to take into account the fact that the voltage for APs at the V_{NE} node typically ranges from tens to hundreds of microvolts in the extracellular recording, whereas that in the intracellular recording is 1~2 orders of magnitude higher [2]; the lower gain for the intracellular recording helps avoid saturation.

The bandwidth of the inverting amplifier [Fig. 3(a), middle] is set to sub-Hz – 5 kHz to cover the spectral range of the electrophysiological signal by adjusting the value of the feedback pseudo resistor R_2 , which consists of 7 antiparallel diode pairs (DPs) and switches [Fig. 3(b), right]. A small leakage current from the DPs in the resistor R_2 to substrate would affect the DC level of the RB amplifier output. To compensate this effect and adjust the output DC level proper, we set in a small anti-current through another pseudo resistor (a DP), R_1 , connected to the negative input terminal of the op-amp, where the anti-current magnitude is determined by R_1 along with the DC biases, V_{b1} and V_{b2} , for the op-amp [20]. The on and off designations for all switches—*i.e.*, S_1, S_2, \dots, S_7 , and the switches in C_2 and R_2 —to set the configuration, gain, and bandwidth of the RB amplifier are stored in latch memory units within each pixel.

Noise is another key consideration in the design of the RB amplifier. Our design is such that the integrated input-referred noise (IRN) (integration bandwidth: sub-Hz to 5 kHz, which is the amplifier bandwidth) is around $\sim 10 \mu\text{Vrms}$ for the extracellular recording mode (gain: 140), which is sufficient given that the AP voltage at the amplifier input (V_{NE} node) is in the range of tens to hundreds of microvolts in the extracellular recording. The IRN for the intracellular recording mode with the smaller gain of 25 then would tend to be larger than that for the extracellular recording mode, but the amplifier input voltage for APs in the intracellular recording mode, which is 1~2 orders magnitude higher than that for the extracellular recording mode, would lie substantially above the increased IRN.

Fig. 3(c) shows the measured gain magnitude vs. frequency of an RB inverting amplifier, the histogram of the measured flat band gain magnitudes for all 1,024 RB inverting amplifiers, the measured IRN power spectral density vs. frequency of an RB inverting amplifier, and the histogram of the measured integrated IRN (integration bandwidth: 0.5 Hz – 5 kHz) for the 1,024 RB inverting amplifiers for both intracellular (green) and extracellular (red) recording scenarios.

B. Detection Block (DB)

Fig. 4(a) shows the schematic of the DB, which serves to detect spikes from the amplified electrophysiological signal— V_{IN} in Fig. 4—arriving from the RB. Since the noise floor of V_{IN} varies with cell types, and from pixel to pixel even for a given cell type, the DB is designed in such a way that it can automatically adjust the spike detection threshold adapted to the noise floor. The design of this spike detector is inspired by Ref. [21].

The spike detection involves two processes: generation of what we call root threshold voltage $V_{t,1}$ based on the noise level

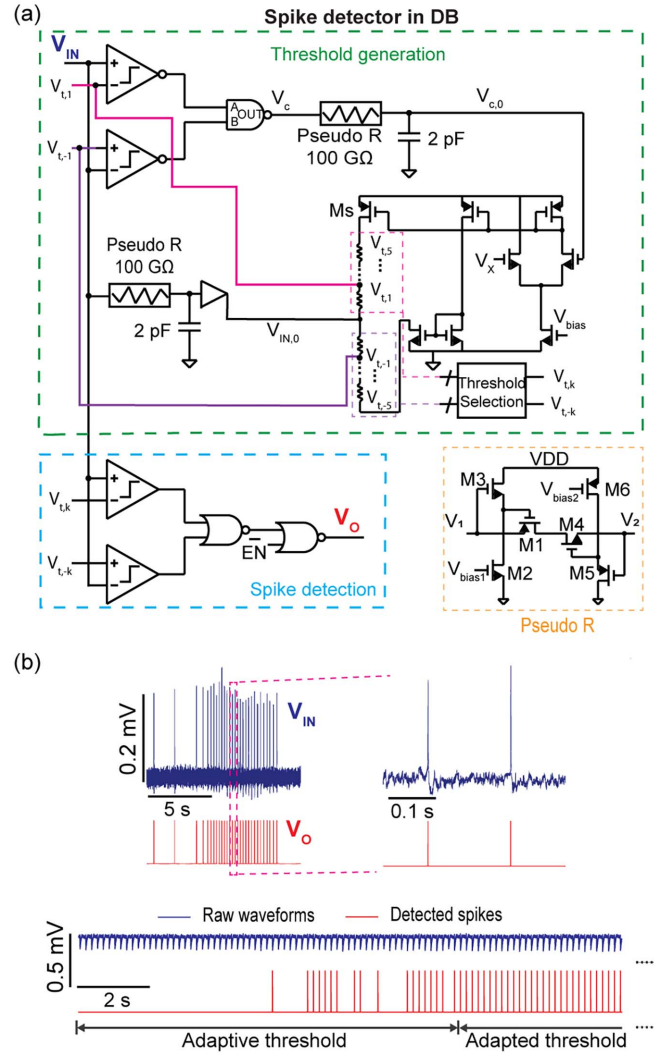


Fig. 4. (a) Schematic of a spike detector. The negative feedback loop inside the green dashed box generates thresholds, and the circuit inside the blue dashed box detects spikes by comparing V_{IN} with one of the generated thresholds. The inset at the bottom right shows the pseudo resistor used in the low-pass RC filters. (b) Top: spike detection with intracellular neuronal recording and $k = 3$ in steady state. Bottom: spike detection with extracellular cardiomyocyte recording and $k = 1$. This measured trace includes the transient towards steady state.

of V_{IN} , and comparison of V_{IN} to this threshold voltage or its variation for spike detection. We describe the two processes in the following two subsections.

1) *Threshold Generation:* The negative feedback loop in the DB, shown inside the dashed green box of Fig. 4(a), generates $V_{t,1}$ based on the noise level of V_{IN} . $V_{t,1}$ takes the form of $V_{t,1} = V_{IN,0} + \alpha$, where $V_{IN,0}$ is the baseline of V_{IN} (*i.e.*, the low-pass filtered V_{IN}) and α is a positive voltage quantity to be determined based on the noise level of V_{IN} . That is, $V_{t,1}$ is set by determining α . In what follows, we explain the machinery of the negative feedback loop to determine α based on the V_{IN} noise level. Throughout the remainder of this subsection (Sec. III.B1), we assume no spikes in V_{IN} , *i.e.*, V_{IN} is assumed to be a pure noise process n on top of the baseline $V_{IN,0}$. This is expressed as $V_{IN} = V_{IN,0} + n$.

Imagine a certain fixed α and the corresponding $V_{t,1} = V_{IN,0} + \alpha$. Inside the dashed green box of Fig. 4(a), $V_{IN} = V_{IN,0} + n$ at a given time is compared to $V_{t,1} = V_{IN,0} + \alpha$ by the top comparator and to $V_{t,-1} \equiv V_{IN,0} - \alpha$ (a variation of $V_{t,1}$) by the bottom comparator. The NAND gate output V_c is then given by:

$$\begin{cases} V_c = 0 & \text{[if } V_{IN} \text{ falls in } (V_{t,-1}, V_{t,1}) \text{ or if } |n| < \alpha] \\ V_c = V_{DD} & \text{[if } V_{IN} \text{ out of } (V_{t,-1}, V_{t,1}) \text{ or if } |n| > \alpha]. \end{cases} \quad (1)$$

As n —and thus V_{IN} —fluctuates over time, let Eq. (1) be satisfied with a probability p and Eq. (2) with a probability $1 - p$ (that is, p is the probability for V_{IN} to fall in $(V_{t,-1}, V_{t,1})$ or for $|n| < \alpha$ and $1 - p$ is the probability for V_{IN} to fall out of $(V_{t,-1}, V_{t,1})$ or for $|n| > \alpha$). The RC filter output, $V_{c,0}$, which is a DC component of V_c , is then given by

$$V_{c,0} = (1 - p) \cdot V_{DD}. \quad (3)$$

Importantly, p depends on α or $V_{t,1} = V_{IN,0} + \alpha$, and so does $V_{c,0}$ according to Eq. (3). Concretely, for a higher α or $V_{t,1}$, a larger p and thus a smaller $V_{c,0}$ results. Moreover, as $V_{c,0}$ is an input to the differential pair in the feedback loop, the smaller $V_{c,0}$ increases the gate voltage of the pMOS transistor M_S atop the resistor string, thus decreasing the string current I_s . In sum, a higher α or $V_{t,1}$ yields a higher p , a lower $V_{c,0}$, and a lower I_s .

We have so far described the operation of the circuit in the green dashed box of Fig. 4(a) without considering the feedback loop, *i.e.*, we have considered a fixed α (thus a fixed $V_{t,1}$) with no account of its update via the feedback. We now consider the feedback loop connecting the top node of the first resistor from the middle point of the resistor string (the string consists of 10 resistors of identical value R_s) to the top comparator. The voltage of this node is just $V_{t,1}$, which does take the form of $V_{t,1} = V_{IN,0} + \alpha$, with the first term arising from the low-pass filtered V_{IN} connected to the string midpoint, and the second term being $\alpha = I_s R_s$, the voltage drop across the first resistor above the string midpoint. There is yet another loop-closing connection, one that is from the bottom node of the first resistor below the string midpoint to the bottom comparator. The voltage of this node is just $V_{t,-1}$, which indeed takes the form of $V_{t,-1} = V_{IN,0} - \alpha$.

For a given intensity of noise n , the closed loop eventually reaches a steady state, with $V_{c,0}$ settling close to V_X , the other (adjustable) input to the differential pair, with the closeness increasing with the differential pair's transconductance. Exploiting this behavior, we can adjust V_X so that α and thus $V_{t,1} = V_{IN,0} + \alpha$ can settle anywhere in the noise level in steady state. For example, if n is a Gaussian noise process with a standard deviation of σ , setting $V_X = 0.32V_{DD}$ leads to $V_{c,0} \approx 0.32V_{DD}$ or $p \approx 0.68$ in steady state, settling α approximately at σ (or $V_{t,\pm 1}$ at $V_{IN,0} \pm \sigma$) due to the property of the Gaussian process. Using this line of argument, we can see that for $V_X < 0.32V_{DD}$, $\alpha > \sigma$ in steady state. In sum, for a given noise intensity, the steady-state $V_{t,\pm 1}$ can be set anywhere in the noise level by an adequate adjustment of V_X (in passing, for a given noise intensity, if $V_{t,1} = V_{IN,0} + \alpha$ were to increase from its steady-state value, I_s is lowered as discussed earlier, decreasing $\alpha = I_s R_s$, and thus reducing back $V_{t,1} = V_{IN,0} + \alpha$; the loop does have a negative feedback).

It is important to note that for a given V_X , if the noise floor of V_{IN} is changed, α —and thus the root threshold voltage, $V_{t,1} = V_{IN,0} + \alpha$ —is automatically adjusted, adapted to the changed noise. For example, again assume a Gaussian noise process and $V_X \approx 0.32V_{DD}$. If σ is changed (*i.e.*, if the noise intensity is changed), α will alter to settle, in steady state, approximately again at the changed σ (or, $V_{t,\pm 1}$ will alter to settle approximately again at the changed $V_{IN,0} \pm \sigma$). This adjustment of the root threshold voltage according to the noise level for a given V_X entails the change of I_s , or the slight $V_{c,0}$ adjustment around $0.32V_{DD}$ by the negative feedback.

In the operation of the pixel array for a given electrophysiological experiment, we apply the same V_X to all 1,024 DBs in the 1,024 pixels. As different V_{IN} signals to the different DBs have different noise floors in general, each DB will settle at its own α , or its own root threshold voltage, $V_{t,1} = V_{IN,0} + \alpha$, adapted to the noise of the V_{IN} signal to the DB. Concretely, in the example of Gaussian noise processes with the identical $V_X \approx 0.32V_{DD}$ applied to all DBs, the steady state α value of each DB will be the σ of the noise of the V_{IN} signal to that DB.

2) *Spike Detection:* Since the resistor string contains 10 resistors of identical resistance R_s with the midpoint biased at $V_{IN,0}$, once the negative feedback loop with a chosen V_X settles α into its steady-state value for a given noise intensity, all the node voltages along the string will also reach their steady-state values given by $V_{t,\pm k} = V_{IN,0} \pm k\alpha$ ($k = 1, 2, 3, 4$, and 5 ; “+” and “-” signs address the nodes in the upper and bottom half of the string) where the $k = 1$ case has been amply discussed. By selecting k , one can choose $V_{t,\pm k}$ as two threshold voltages to feed to the comparators inside the blue dashed box of Fig. 4(a), so that V_{IN} can be compared with them for spike detection. In this context, V_{IN} contains spikes as well as noise. If a spike peaks above $V_{t,k}$ or dips below $V_{t,-k}$ (*i.e.*, if the spike magnitude is larger than $k|n|$), the two comparators followed by the digital logic [Fig. 4(a), blue dashed box] will produce a digital pulse at the moment of the spiking, which registers as the DB's output, V_O .

A higher k value gives a higher threshold, thus a stricter criterion for spike detection. We typically set k to 3 or 4 with $V_X \approx 0.32V_{DD}$ for intracellular recording, as the intracellular recording has a higher signal-to-noise ratio (SNR). For extracellular recording with a lower SNR, we usually set k to 1 or 2. In this case of using lower k values, we set V_X lower than $0.32V_{DD}$ so that $\alpha > \sigma$ holds in steady state. This is to minimize the chance that noise itself generates spurious digital pulses.

Fig. 4(b), top, shows an experimental demonstration of spike detection in a pixel in steady state (*i.e.*, after α settles) with an intracellular neuronal recording and $k = 3$. Fig. 4(b), bottom, is another measurement of pixel spike detection, this time with an extracellular cardiomyocytes recording and $k = 1$. This second measurement shows the transient that settles to a steady state with a high initial α . Thus no spike detection occurs initially. But as the circuit evolves toward the steady state with α lowered, increasingly more spikes are detected. In steady state, all spikes are sensed (we note that these electrophysiological recordings in Fig. 4(b) are done after post-fabricating particular electrode structures on the CMOS chip, which we will discuss in Sec. IV).

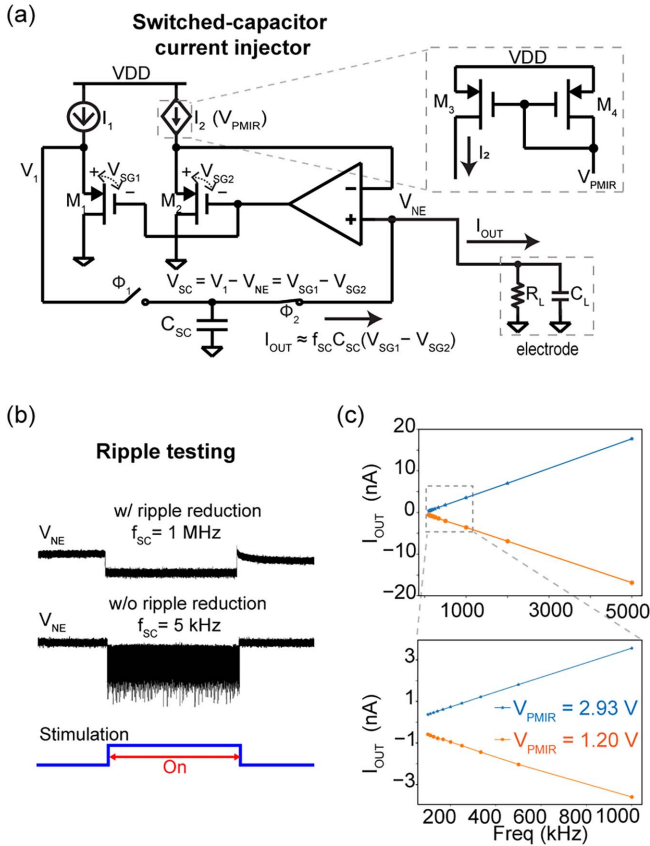


Fig. 5. (a) Switched-capacitor current injector topology. (b) Experimental verification of ripple removal with a high enough f_{SC} (1 MHz). (c) I_{OUT} versus f_{SC} for two different values of V_{PMIR} . The inset shows the current range used in our electrophysiological experiments.

C. Stimulation Block (SB)

C1) Design and Characterization: The SB of a pixel injects a current to the electrode in the pixel for cell stimulation. It contains two current injectors in parallel, one producing I_{STIM} and the other I_{HOLD} [Fig. 2(a)]. The SB thus can inject a total current of $I_{STIM} + I_{HOLD}$ to the pixel electrode. The two current injectors share the same switched-capacitor circuit topology of Fig. 5(a) and have the same operating principle, while they can be independently controlled. We will now explain the operating principle of the current injector topology, calling its injection current I_{OUT} generically, which can be either I_{HOLD} or I_{STIM} .

The topology employs two pMOS transistors, M_1 and M_2 , an op-amp in a negative feedback, and a capacitor C_{SC} that is switched at a frequency of f_{SC} between two voltages, V_1 and V_{NE} shown in Fig. 5(a), with the latter being the electrode voltage. I_{OUT} injected to the electrode is then given by $f_{SC} \times C_{SC} \times (V_1 - V_{NE})$ according to the principle of the switched capacitor. At the same time, the negative feedback by the op-amp enforces $V_1 - V_{NE} = V_{SG1} - V_{SG2}$ where V_{SG1} and V_{SG2} are the source-gate voltages of M_1 and M_2 . Therefore, the injected current can be re-expressed as $I_{OUT} = f_{SC} \times C_{SC} \times (V_{SG1} - V_{SG2})$.

Based on this current injection formula, we can observe several benefits of this current injector topology. First, I_{OUT} depends neither on V_1 alone nor V_{NE} alone, but on $V_1 - V_{NE}$, or equivalently $V_{SG1} - V_{SG2}$. Therefore, the current injector has a

high output impedance, and can inject a prescribed current regardless of the V_{NE} variation the injection may cause. Second, by adjusting V_{SG1} and V_{SG2} via the bias currents of M_1 and M_2 , we can obtain both positive and negative polarities in I_{OUT} . Third, again by adjusting V_{SG1} and V_{SG2} , we can make $|V_{SG1} - V_{SG2}|$ sufficiently small to obtain a target I_{OUT} with a switching frequency f_{SC} sufficiently above the spectral range of the electrophysiological signals; this ensures that ripples associated with the switched capacitor can be readily filtered out by the RB amplifier, whose bandwidth more or less matches the spectral range of the electrophysiological signal. Fourth, I_{OUT} tuned by the frequency f_{SC} can achieve a wide tuning range (0–20 nA).

In developing this current injector topology, we started from the basic ideas in our earlier switched-capacitor current injector topology used in Ref. [2] and detailed in Ref. [20]. However, the present topology represents a substantial design upgrade, with the key improvement being the third benefit mentioned above, that is, the ability to obtain a target I_{OUT} while filtering out the ripples from the switched capacitor. Fig. 5(b) shows measurements demonstrating this third benefit, where we compare the cases of $f_{SC} = 5$ kHz and $f_{SC} = 1$ MHz, with each injecting ~ 1 nA via respective adjustment of $V_{SG1} - V_{SG2}$. For $f_{SC} = 5$ kHz, an appreciable ripple is observed in the signal recorded by the RB amplifier [we remind readers that the RB amplifier gain rolls off to below 1 at frequencies in excess of 10 kHz; Fig. 3(c)], which is referenced back to the V_{NE} (amplifier input) node in Fig. 5(b). By contrast, for $f_{SC} = 1$ MHz, which is well beyond the bandwidth of the RB amplifier, the ripple is quite suppressed in the recorded signal. This attests to the benefit of tuning $V_{SG1} - V_{SG2}$ small enough and thus setting f_{SC} high enough to produce a target current with minimal ripples.

$V_{SG1} - V_{SG2}$ is adjusted by the voltage V_{PMIR} (generated by off-chip auxiliary electronics (digital-to-analog converter) on a printed circuits board (PCB); see Section IV-B for experimental setup), which controls the bias current of transistor M_2 [Fig. 5(a)]. Fig. 5(c) shows measured I_{OUT} vs. f_{SC} for two differing V_{PMIR} values. This shows that the magnitude of I_{OUT} increases with f_{SC} , and its polarity can be selected by V_{PMIR} .

C2) Operation in an Electrophysiological Experiment: As mentioned earlier, the two current injectors of a pixel SB, which produce I_{HOLD} and I_{STIM} , are of the same topology of Fig. 5(a), and the generically-called I_{OUT} can be I_{HOLD} or I_{STIM} . Therefore the polarity and magnitude of I_{HOLD} and those of I_{STIM} can be controlled separately by each current injector's V_{PMIR} and f_{SC} . The polarity and magnitude of the total current $I_{HOLD} + I_{STIM}$ are then accordingly determined. In a destination (stimulation) pixel in a closed-loop experiment, the configuration signals from EPs are used to turn on and off I_{STIM} , controlling the timing and the duration of each I_{STIM} pulse to manipulate the behaviors of a cell or cells coupled to the destination pixel.

It is important to note that a pixel can *simultaneously* perform voltage recording with its RB block and a current injection with its SB block (in this connection, note in Fig. 2 that in each pixel, the SB output, the RB input, and the electrode are all directly connected with no switch). This is a useful feature. For example, in a destination pixel, when I_{STIM} controlled by a configuration

signal from an EP is applied to stimulate cells, the pixel can also concurrently record the cells' electrophysiological voltage signals to measure the effect of the stimulation. For another example, in a recording pixel, simultaneous voltage recording and sustenance of a negative current injection—with the magnitude up to a few nA—can enable, albeit not guaranteeing, intracellular voltage recording, if certain electrode structures are employed [2], [20]. We can use, for example, I_{HOLD} for the negative current injection to help enable intracellular recording. All previously mentioned intracellular recordings were (and intracellular recordings to be seen later are) achieved in this way.

Up to a few nA of current in magnitude is injected into an electrode for both stimulation and intracellular access [2]. The electrode impedance ranges from tens to hundreds of k Ω , depending on the electrode structure and surface treatment, so the voltage drop across the electrode during current injection is negligible (for cell-electrode interface impedances, which are particularly relevant for intracellular coupling, we refer readers to our earlier work in Ref. [2]; while using a different chip, it would offer a feel). In our electrophysiological experiment, we do not necessarily pursue charge balancing during current injection into an electrode. A case in point, to attain and maintain an intracellular access, as briefly mentioned earlier, we need to inject a negative current—or we so far only know this particular current injection method for intracellular access. Finding a way to help reduce electrode degradation in this context, thus, may have to be further researched.

D. Event Processor (EP)

The CMOS chip contains 10 EPs, whose operation we detail in this subsection. For the time being, we consider a single EP forming a closed loop with a single recording pixel and a single destination (stimulation) pixel, in connection with Fig. 6(a), which presents the schematic and timing diagram of the EP. The EP receives a stream of digital pulses representing detected spikes from the DB of the recording pixel, and issues configuration signals in the form of digital pulses to the SB of the destination pixel to instruct the timing and duration of each I_{STIM} pulse. Concretely: a delay T_1 between an input pulse representing a detected spike and a pulse in a configuration signal signifies how long a destination pixel should wait to inject a I_{STIM} current after a spike is detected in the recording pixel; a duration T_2 of the pulse in the configuration signal dictates how long the I_{STIM} current injection in the destination pixel should last; finally a deadtime T_3 following the pulse in the configuration signal is the duration over which no I_{STIM} current injection must be made. With T_3 , not every input spike pulse needs to produce a pulse in the configuration signal, which serves to prevent overstimulation. T_1 , T_2 , and T_3 are programmable independently.

To accomplish the abovementioned functionality, the EP is constructed with an input latch followed by three sequentially connected digital modules, A, B, and C [Fig. 6(a)]. The input latch converts an input digital spike pulse into a step function. Modules A, B, and C have exactly the same logic circuit [Fig. 6(b)]. This logic circuit, which contains a 10-bit counter and a 10-bit digital comparator, takes a step function input (IN) to

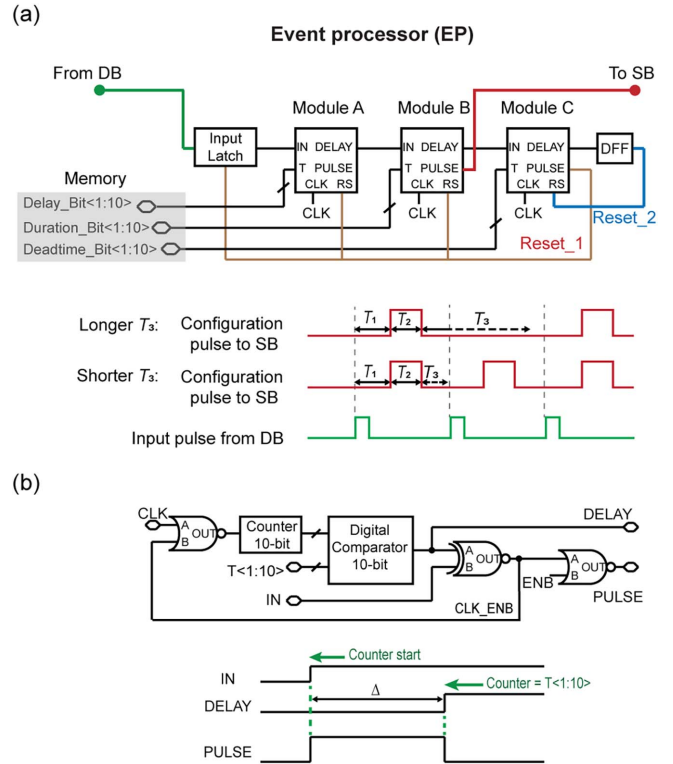


Fig. 6. (a) Schematic and timing diagram of an EP. (b) Schematic and timing diagram of a digital module in an EP.

generate two outputs: a delayed step function (DELAY) and a square pulse (PULSE). Here the delay Δ between the two step functions is equal to the duration of the square pulse. Δ is programmable. Since DELAY of module A serves as IN of module B, PULSE of module B serves as the output of the EP, and PULSE of module C resets the input latch, it can be checked by inspecting timing diagrams along the chain of the input latch and the three modules that the Δ of module A serves as T_1 , the Δ of module B serves as T_2 , and the Δ of module C serves as T_3 . All of these three times are independently programmable with a 10-bit control. Each time parameter has a control resolution corresponding to one period of the clock (CLK) signal, and can accommodate up to 2^{10} clock periods. With this arrangement together with the tunability of the clock frequency that can exceed 1 MHz, each of T_1 , T_2 , and T_3 can be tuned from zero to seconds with a tuning resolution of sub-microseconds.

Fig. 7(a) shows oscilloscope traces of the RB and DB outputs of a recording pixel, the configuration signal (SB input), and injected current in a destination pixel, where the recording and destination pixels are connected via an EP with $T_1 = T_2 = 10$ ms and $T_3 = 0$. For this measurement, we apply a 5-ms artificial pulse input—not shown in the figure as the oscilloscope can track only 4 traces—to the recording pixel. The measured traces show that the DB registers the RB output as a spike, the EP generates a configuration pulse with the programmed T_1 and T_2 , and a current is injected according to the configuration pulse.

While we have so far described the simplest closed-loop where a single recording pixel and a single destination pixel are connected via a single EP for simplicity, the closed-loop can be

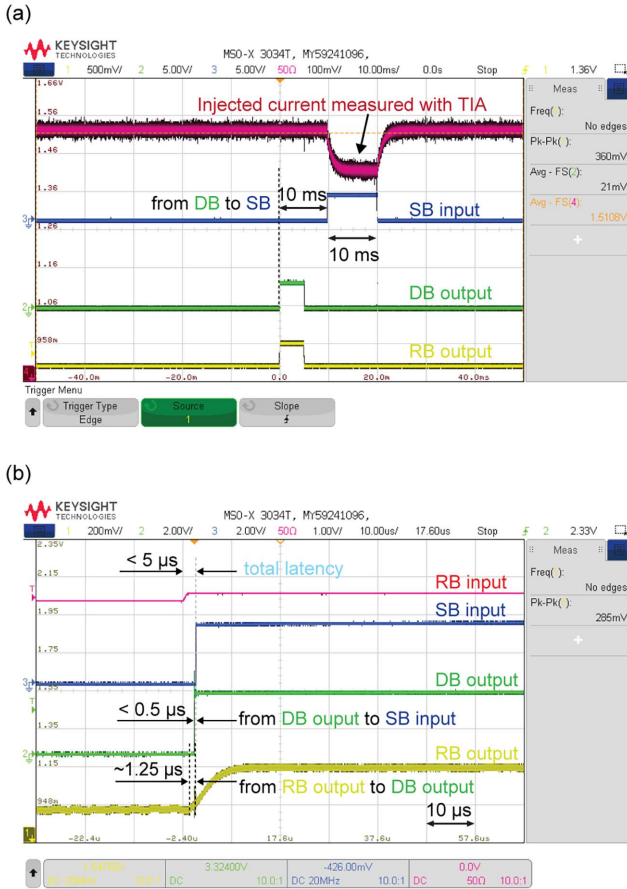


Fig. 7. (a) Oscilloscope traces of the RB and DB outputs of a recording pixel, the configuration signal (SB input), and the injected current in the destination pixel, with the two pixels linked via an EP with $T_1 = T_2 = 10$ ms and $T_3 = 0$. Here we apply a 5-ms artificial pulse input, not shown in the figure, to the recording pixel. (b) Oscilloscope traces verifying that the RB-DB-EP-SB path has an intrinsic latency quite less than 5 μ s. For this measurement, we set $T_1 = 0$.

much more comprehensive in connecting pixels. Concretely, each recording pixel can send spike detection results to any of the 10 EPs simultaneously, and each destination pixel can receive configuration signals from any of the 10 EPs simultaneously. Furthermore, each EP can receive input spike pulses from any of the 1,024 pixels simultaneously and can issue configuration signals to any of the 1,024 pixels simultaneously.

Finally, in the integrated closed-loop operation, the intrinsic parasitic delay, *i.e.*, the delay in addition to the intended T_1 , from an input in a recording pixel to a current injection in a destination pixel via the RB-DB-EP-SB path is quite less than 5 μ s—which is negligible in the time scale of electrophysiological dynamics—as seen in the measurement of Fig. 7(b) with $T_1 = 0$. In this measurement, we input a large signal to show a clear rising edge and to avoid saturation, we use the RB amplifier in a non-inverting, unity-gain configuration thus with a larger bandwidth, as compared to the inverting configuration with the larger gain (25 or 140) and a smaller bandwidth used in the actual electrophysiological work. This arrangement, however, hardly hinders us from measuring a reasonable approximation for the parasitic delay in the actual operational mode, as the bandwidth already plays a negligible role in determining the delay in the

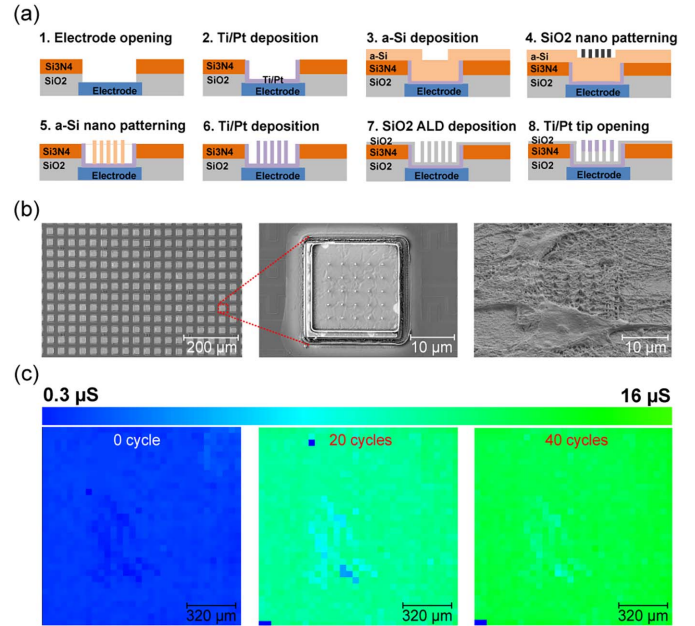


Fig. 8. (a) Electrode post-fabrication steps. (b) SEM images of the electrode array on the CMOS chip and a neuronal culture on top. (c) Conductance heat maps across the electrode array at 0, 20, and 40 cycles of electrodeposition.

actual operational mode, with the spectral contents of electrophysiological signals falling within its bandwidth.

IV. ELECTRODE FABRICATION, EXPERIMENTAL SETUP, AND ELECTROPHYSIOLOGICAL RECORDING

Section III has described the design and electrical characterization of the CMOS IC itself, which we designed and a silicon foundry fabricated. We now discuss the development of the CMOS electrode array from the foundry-fabricated CMOS chip, and electrophysiological recording experiments with it.

A. Electrode Post-Fabrication on the CMOS Chip

The center area of the foundry-fabricated CMOS chip features $32 \times 32 = 1,024$ metallic pixel pads on its surface [Fig. 1(b)], each of which is connected to its own AFE unit containing the RB, DB, and SB. On each pixel pad we post-fabricate, in house, 5×5 vertically standing nanoelectrodes [Fig. 1(b), top right; Fig. 8(a), 8(b)] using a top-down fabrication process [2]. Each vertical nanoelectrode consists of a vertically standing SiO₂ core, a thin Ti/Pt coating on this core, and another SiO₂ insulation layer on the lower part of the Ti/Pt coating. The Ti/Pt metal exposed at the higher part of the vertical structure serves as an electrode. Note that the 25 nanoelectrodes per pad are all shorted together on the pixel pad, and thus electrically they act as one effective electrode (so the chip features a total of 1,024 effective electrodes even after post-fabrication). The vertical nanoelectrodes in conjunction with a negative current injection allow for intracellular recording, while they can also perform standard extracellular recording with no current injection [2]. Once post-fabricated, the CMOS electrode array is packaged in a chip carrier and bonding wires are encapsulated by pouring polydimethylsiloxane (PDMS) between two glass rings [Fig.

1(b), bottom] [2]. The outer glass ring also serves to hold cell culture media.

Following the packaging, we perform electrodeposition of Pt black (PtB) on the Ti/Pt electrodes to increase their surface area and thus conductance, before we engage the chip for electrophysiological recording. For the PtB deposition, a solution of 0.5 mM H_2PtCl_6 and 25 mM NaNO_3 is held inside the outer glass ring, and the CMOS electronics is used to scan the electrode voltage from 0 V to -1.2 V relative to a Pt reference electrode at a scan rate of 50 mV/s for 10 to 60 cycles (while we have so far discussed only the current injection and voltage recording capability of the AFE units, they can be reconfigured to apply voltages to their connected electrodes). The simultaneous measurement of the electrode current using an off-chip transimpedance amplifier (TIA) confirms that the PtB coating increases the electrode conductance (e.g., in Fig. 8(c), the conductance increases from sub μS to 16 μS after 40 cycles).

B. Experimental Setup

Fig. 9(a) shows the experimental setup for the CMOS chip, used for both the characterization of the CMOS chip and electrophysiological work. The chip is mounted on a PCB, which also hosts a Verilog-programmed FPGA. The FPGA is interfaced with a Python-based graphical user interface (GUI) in a personal computer (PC). The FPGA, which is the traffic hub for both digitized data and digital control signals on the PCB, coordinates the operation of the PCB and the CMOS chip. The PCB also includes analog-to-digital and digital-to-analog converters.

Now more in details, both RB and DB outputs are routed, via multiplexing, to the PCB and then to the PC, where the GUI visualizes the electrophysiological recording data and spike detection data in real time to confirm the capability of the CMOS chip to record electrophysiological signals and to detect spikes. The GUI also allows for adjusting and optimizing the circuit parameters on the fly based on the real-time electrophysiological recording and spike-detection data. The off-chip reference electrode current is measured by the aforementioned TIA on the PCB, which is also monitored in real time by the GUI. Finally, the PCB also includes an LDO, a digital isolator, and a PID controller for power and noise management of the PCB and the temperature management of the CMOS chip via the on-chip heater and temperature sensor. This experimental setup of Fig. 9(a) for data acquisition and user interaction in real time is much smaller than commercial data acquisition systems. Fig. 9(b) presents a number of photos for the experimental setup.

C. Electrophysiology Recording

For neuronal recording, we culture rat neurons, a combination from the cortex, hippocampus, and ventricular zones, on the CMOS electrode array (1.5×10^5 cells within an area of $5 \text{ mm} \times 5 \text{ mm}$ at and around the center of the chip). For cardiomyocyte recording, we culture dissociated rat whole heart on the CMOS electrode array (0.7×10^5 cells within the same area mentioned above). Both neurons and cardiomyocytes are procured from Transnetyx Tissue by BrainBits. Prior to each cell plating, the CMOS chip is coated with poly-D-lysine (PDL) to

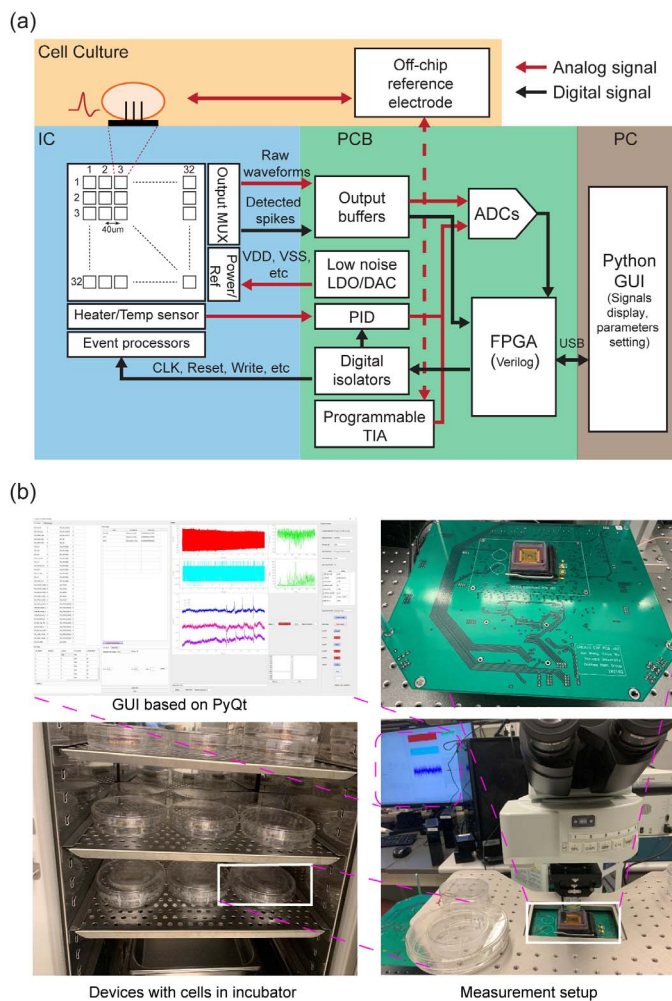


Fig. 9. (a) The CMOS IC operating setup. (b) Packaged CMOS electrode array chips with cells plated on top are stowed in an incubator for cell culture. For electrophysiological recording, the packaged CMOS electrode array chip is mounted on the PCB, which is installed in a probe station with an optical microscope.

promote neuron attachment and with Gelatin to promote cardiomyocyte attachment to its surface. Typically, rat neurons begin to show activity around 14 days in vitro (DIV). We usually perform electrophysiological recordings during DIV 20 to 30, when the cells exhibit peak activity levels. Rat cardiomyocytes start to beat and generate electrical signals around DIV 7. By DIV 14, they form a cohesive cell sheet and tend to synchronize their beating. The recording from cardiomyocytes presented in this work are conducted after DIV 14.

Fig. 10 shows example extracellular (top) and intracellular (bottom) recording of membrane potentials by the CMOS electrode array for neuronal and cardiomyocyte cultures on the chip. APs or spikes clearly manifest in all four cases in Fig. 10. The intracellular recording is enabled by a negative current injection (Sec. III.C), whereas the extracellular recording is done without current injection. The intracellular recording has a far greater SNR (especially in the case of neurons), while the extracellular recording can last much longer due to its non-invasiveness. This set of measurements attests to the ability of the CMOS electrode array to form electrical interfaces with biological cells.

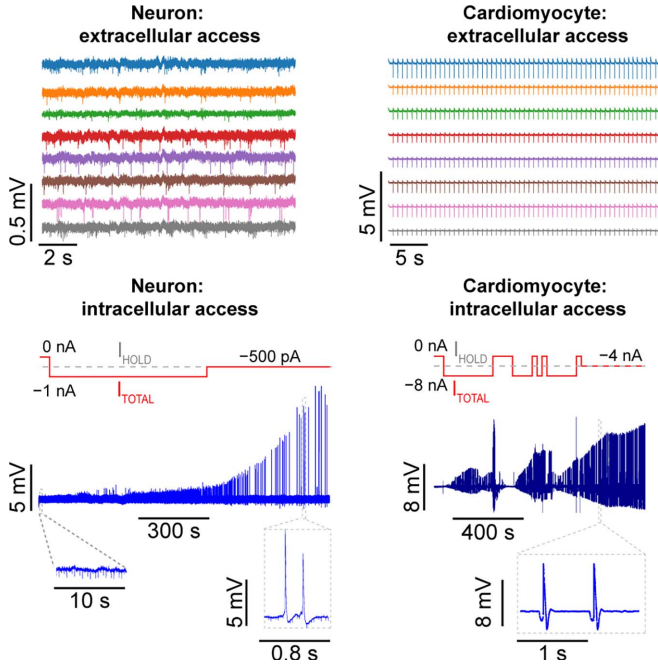


Fig. 10. Top: extracellular recording traces for rat neurons and cardiomyocytes. Bottom: intracellular recording traces shown together with injected current waveforms for rat neurons and cardiomyocytes.

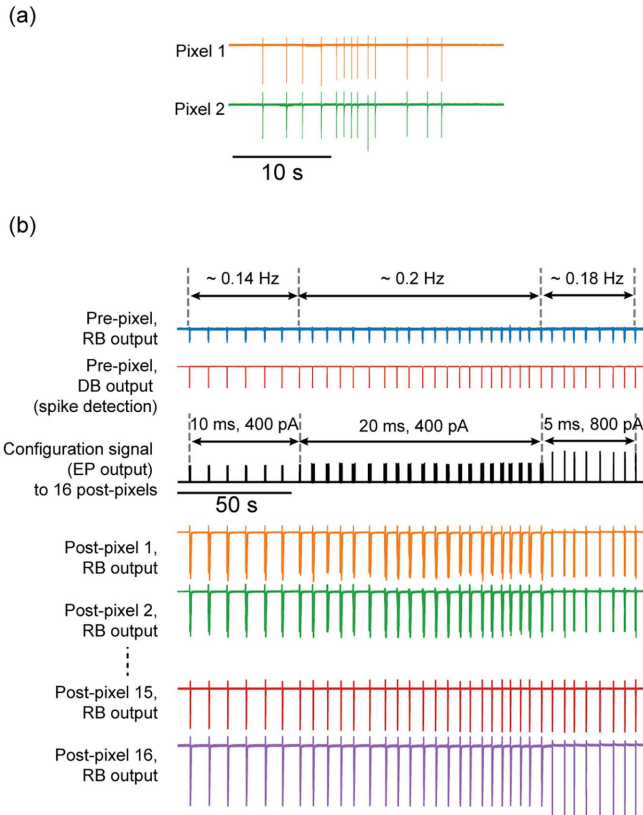


Fig. 11. CMOS-cardiomyocytes extracellular interface. (a) Spontaneous synchronous oscillations of cardiomyocytes in the absence of stimulation by the CMOS electrode array. (b) Electrophysiological activities recorded at 1 pre-pixel and 16 post-pixels with closed-loop modulation pathways activated between the single pre-pixel and the 16 post-pixels (stimulation artifacts are overlapped with cell activities). The configuration signal, sent by an EP to the 16 post-pixels, is also shown.

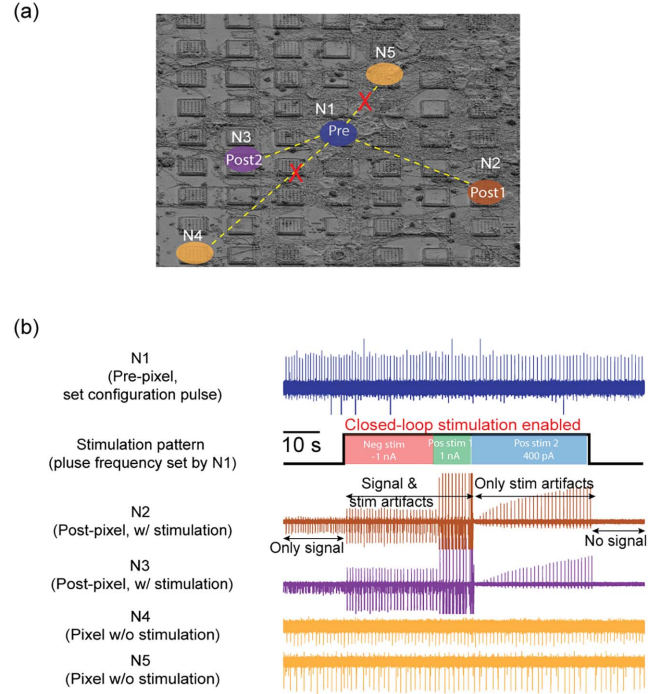


Fig. 12. Closed-loop modulation experiments with neurons. (a) 5 pixels involved in our measurements are shown. (b) Recorded voltage waveforms from the 5 pixels (N1~N5), and stimulation pattern with frequency set by N1 and polarity labelled during closed-loop stimulation.

V. CLOSED-LOOP MODULATION EXPERIMENTS

We now present closed-loop modulation experiments. We start with a tissue of cardiomyocytes cultured on the CMOS electrode array. The bio-semiconductor interface in this case is of extracellular nature. In Fig. 11(a), extracellular recording performed by the CMOS chip with no stimulation applied reveals a spontaneous oscillation of the cardiomyocyte network, where spikes appear synchronously at different pixels. For the measurement in Fig. 11(b), we turn on closed-loop modulation pathways from 1 source pixel (referred to as ‘pre-pixel’ in the figure) to 16 destination pixels (referred to as ‘post-pixels’, with select 4 displayed in the figure). For this experiment, we set $T_1 = 0$ and $T_3 = 100$ ms (T_2 is variable), so that every spike detected in the pre-pixel leads to nearly immediate I_{STIM} current injections in the 16 post-pixels ($I_{HOLD} = 0$ throughout this experiment). As seen in Fig. 11(b), in this closed-loop configuration, recording traces of the 17 pixels—the pre-pixel performs voltage recording only, but each of the 16 post-pixels performs current stimulation and voltage recording simultaneously—exhibit synchronous oscillation initially at a frequency of 0.14 Hz with $T_2 = 10$ ms and $I_{STIM} = 400$ pA (*i.e.*, a current of 400 pA is injected in each of the 16 post-pixels for 10 ms whenever a pre-pixel detects a spike), but as we tune (T_2 , I_{STIM}) to (20 ms, 400 pA) and then to (5 ms, 800 pA), the synchronous network oscillation frequency changes to 0.2 Hz and then to 0.18 Hz. The closed-loop bioelectronic interface thus is a self-sustained cyto-silicon hybrid oscillator, where not only the cells and CMOS feedback pathways exhibit the same rhythmic dynamics locked together but the artificial feedback via the CMOS IC influences the synchronous network oscillation frequency.

TABLE I
COMPARISON WITH OTHER RELEVANT WORK

		This Work	[1] Frontiers in Neural Circuits 2012	[7] Nature BME 2023	[15] TBioCAS 2017	[16] JSSC 2017	[17] TBioCAS 2021	[18] JSSC 2022	[22] TBioCAS 2023
Technology (nm)		180	600	N/A	180	130	180 BCD	65	180
Recording	No. Ch	1024	126	32	16	64	8	256	93
	Extracellular recording	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Intracellular recording	Yes	No	No	No	No	No	No	No
Stimulation	No. Ch	1024	42	N/A	16	64	8	16	N/A
	Type	I (0 ~ 20 nA) & V (0 ~ 3.3 V)	I (5 ~ 10 μ A)/V (0.1 ~ 1 V)	Optical	I (0 ~ 4 mA)	I (10 ~ 1350 μ A)	I (0 ~ 12 mA)	I (65 ~ 600 μ A)	Visual
	Polarity	Mono/bipolar	Mono/bipolar	N/A	Mono/bipolar	Mono/bipolar	Bipolar	Bipolar	N/A
	No. sources	10 on-chip (I) + 3 external (V)	2 on-chip	N/A	16 on-chip	64 on-chip	8 on-chip	16 on-chip	N/A
	Resolution	I (continuous) + V (16-bit)	10-bit	N/A	6-bit	8-bit	8-bit	N/A	N/A
Coupling mode		AC & DC	AC	N/A	AC	DC Rail-to-Rail	AC	AC	AC
Bandwidth (Hz)		<1 ~ 5 K	0.5 ~ 10 K	300 ~ 20 K	0.3 ~ 7 K	0.01 ~ 500	0.1 ~ 1 K	1 ~ 500	300 ~ 1000
Gain (V/V)		1 ~ 140	1 ~ 1000	N/A	100	-	5 ~ 158	108 ~ 785	-
IRN (μ V _{rms})	Full band	24.2	11	N/A	4.57	1.13	2.16	3.2	-
	AP band	9.9	N/A	N/A	N/A	-	1.8	N/A	-
On-chip spike detection		Yes	No	No	Yes	No (LFP)	Yes	No (LFP)	Yes
	Thresholds	Adaptive	-	-	6-bit, energy extraction	Phase synchrony	Classification	Biomarker extraction	Spiking band power
Closed-loop	On/Off-chip	On-chip	Off-chip FPGA	Software on PC	On-chip	On-chip	Multi ICs	On-chip	Off-chip
Minimum latency		< 5 μs	Sub ms	Tens ms	Sub ms	N/A	< 0.3 s	< 1 s	N/A

Fig. 12 illustrates a closed-loop modulation (intracellular recording, extracellular stimulation) with rat neurons cultured atop the CMOS chip. Fig. 12(a) shows the SEM image of the electrode array on the CMOS chip surface with neurons cultured to show the position of pixels involved (the actual cell culture used for this experiment is much more densely populated, whereas the cell culture in Fig. 12(a) is separately prepared not for recording but for the SEM imaging with cells less densely plated, dehydrated, and fixed). We establish closed-loop pathways from one recording pixel (N1, called ‘pre-pixel’) to two destination pixels (N2 and N3, called ‘post-pixels’). Fig. 12(b) displays the recorded voltage waveforms from neurons in this closed-loop modulation experiment. In N1, I_{HOLD} is sustained at -1 nA to attain an intracellular recording. In each of N2 and N3, I_{HOLD} is disabled, but a set of I_{STIM} current pulses with variable amplitude and with timing and duration controlled by the configuration signals based on the recording from N1 ($T_1 = 2$ ms, $T_2 = 20$ ms, $T_3 = 100$ ms) are applied. These artificial pathways do not influence the spontaneous activities in N2 and N3 when the current injections in response to N1’s activities are negative (-1 nA). However, positive current injections (both 1 nA and 400 pA) in response to N1’s activities effectively suppress the spontaneous

activities of N2 and N3, thereby creating an artificial inhibitory pathway between the pixels (N1 to N2 and N1 to N3) through the CMOS chip. Meanwhile, two pixels, N4 and N5, which are not integrated in the closed-loop signal pathways, remain unaffected.

VI. CONCLUSION

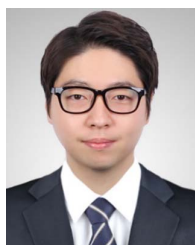
We developed a bioelectronic interface combining biological electrogenic cells and a CMOS electrode array chip with the latter providing on-chip artificial signal pathways between cells. Table I compares this work with other relevant studies to highlight the advance made by our work in this line of bioelectronic interface, in particular, the larger number of recording/stimulation channels and the intrinsic latency of the artificial signal pathway less than 5 μ s. Furthermore, as concrete examples of this cyto-silicon hybrid, we developed a silicon-cardiomyocyte self-sustained oscillator with a tunable locked frequency, and a silicon-neuron interface with silicon inhibitory connection pathways between neurons. Further developments along this direction may one day become useful for prosthesis and brain-machine interface, and also for fundamental investigations such as network-scale modulation of synaptic plasticity.

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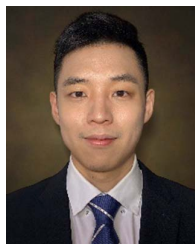
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