

Fully Monolithic 18.7GHz 16Ps GaAs Mode-Locked Oscillators

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Abstract—We report a mode-locked electrical oscillator fully integrated in GaAs. It self generates a periodic train of pulses with a 16-ps pulse width and a 18.7-GHz frequency. This is the fastest electrical mode-locked oscillator to date, and the first integration of reflective mode-locked electrical oscillator. It works by sending a pulse back and forth on a coplanar waveguide with reflections at both ends. The reflection occurs with level-dependent gain that enables pulse formation and stabilization.

Index Terms—Oscillators, mode-locked oscillators, pulse generators, radio frequency, integrated circuits.

I. INTRODUCTION

Mode-locked electrical oscillators periodically burst out a short-duration electromagnetic (voltage and current) pulse [1]–[6]. The periodic train of pulses corresponds to multiple harmonic modes, whose phases have a fixed relationship, or are ‘locked’ to one another. Due to their short pulse duration and inherent short-term frequency stability [7], the mode-locked oscillators can be potentially powerful tools in time-domain metrology, high-speed sampling, and injection-lock based frequency synthesis [8]–[11].

Mode-locked oscillators are classified into two types, circulatory and reflective. In the circulatory type [1]–[4], a pulse circulates in a loop consisting of an electromagnetic waveguide (*e.g.*, a transmission line) and an amplifier. The amplifier provides an overall gain for sustenance of the pulse oscillation. In the reflective type [5], [6], a pulse travels back and forth on an electromagnetic waveguide, reflected at both ends of the waveguide by deliberate impedance mismatches. The pulse oscillation is sustained by incorporating an overall gain in the reflection process.

The concept crucial to any mode-locked oscillator, circulatory or reflective, is *level-dependent gain* [1]–[6]. That is, the aforementioned overall gain actually consists of amplification for a signal beyond a certain threshold and attenuation for a signal below the threshold (overall, there is gain to compensate loss in the system). This level-dependent gain is key to pulse formation and stabilization.

The 1955 invention of the mode-locked electrical oscillator by Cutler [1] precedes the optical mode-locking (pulsed lasers). Despite the early start, works on mode-locked electrical oscillators have been largely focused on proving concept with discrete-level design rather than increasing speed performance with integrated design. Integrated mode-locked oscillators appeared in two recent works [3], [4], both circulatory types, where the latter with a pulse repetition rate

of 8.6 GHz and a pulse width of 42 ps has been the highest-speed mode-locked electrical oscillator so far. Given the potential usefulness of the mode-locked oscillators, it would be valuable to push their speed via integrated circuit design. Implementation at high frequencies offers an interesting radio-frequency integrated circuit design and measurement problem.

This paper reports a fully monolithic mode-locked oscillator, integrated in GaAs technology with metamorphic HEMTs (GaInAs/InAlAs). This represents the first integration of reflective-type mode-locked oscillators [5], [6]. Moreover, its pulse width of 16 ps and pulse repetition rate of 18.7 GHz represent the highest-speed electrical mode-locked oscillator of any type to date, motivating future efforts in high-speed electrical mode-locking. Sec. II explains the topology and operation. Sec. III reports measurement results that attest to the validity of the design.

II. TOPOLOGY AND OPERATION

The mode-locked oscillator, which is of the reflective type as in the discrete-level works [5], [6], is topologically shown in Fig. 1. It combines a transmission line with what we call reflection amplifier and an output buffer.

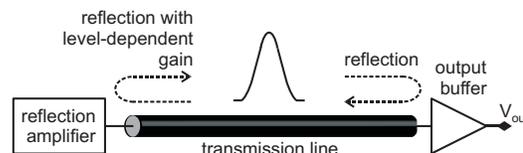


Fig. 1. Topology of the mode-locked oscillator.

In steady state, a pulse travels back and forth on the line, reflected at both line ends by deliberate impedance mismatches. The reflection amplifier presents a negative output resistance for a signal beyond a particular threshold and a positive output resistance below the threshold. Therefore, the portion of an oncoming pulse that lies above the threshold is reflected with gain, while the portion below the threshold is attenuated. This corresponds to level-dependent gain, which forms and stabilizes the pulse. The output buffer at the other line end presents to the line an impedance far larger than the line’s characteristic impedance (thus the oncoming pulse is fully reflected back), while regenerating the pulse with a gain of ~ 0.5 to its $50\text{-}\Omega$ load from the measurement system.

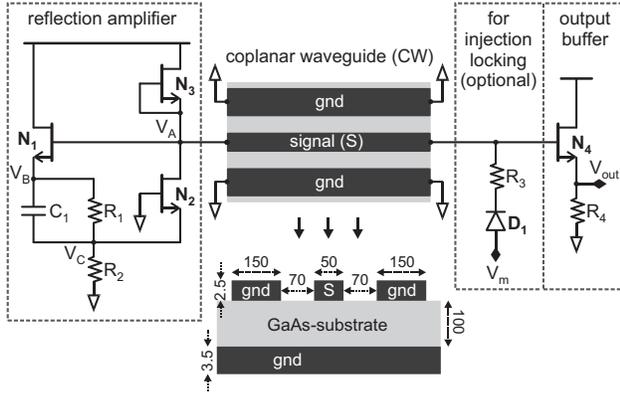


Fig. 2. Schematic of the mode-locked oscillator. All transistors are depletion-mode ones. $C_1=0.55$ pF, $R_1=125$ Ω , $R_2=12.5$ Ω . The dimensions in the CW cross sectional view are in μm 's.

We now explain its operation in detail, using the oscillator schematic of Fig. 2. To begin with, the transmission line is implemented as a 2.4-mm long coplanar waveguide with an added ground plane. Its top and cross sectional views are in Fig. 2, where the dimensions are in μm 's. The coplanar waveguide has a characteristic impedance of 55 Ω and a quality factor of 36 at the pulse repetition frequency of 18.7 GHz, where the frequency is set by the round trip time of the pulse, or the length of the line. Since the GaAs substrate has a very high resistance, the quality factor is determined largely by the metallic loss due to the skin effect.

In steady state, the level-dependent gain is a necessity for pulse shaping and stability. By contrast, initial start-up needs a full gain rather than the level-dependent gain, as the latter would prevent start-up by suppressing small perturbations (*e.g.*, ambient noise), which should actually be promoted for the start-up. The circuit of Fig. 2 is designed to have the adaptive dynamics, where the reflection amplifier provides a full gain during initial start-up and a level-dependent gain in steady state. We now explain the machinery of the adaptive dynamics.

In the initial start-up, the bias of the reflection amplifier is such that gate-source voltages of transistors N_1 and N_2 are both ca. -0.2 V, turning on both N_1 and N_2 , which are depletion-mode transistors. These two turned-on transistors form a positive feedback loop. Consequently, the amplifier's output resistance at the node shown with V_A in Fig. 2 is negative. Therefore, the initial small oscillation that starts forming on the line are reflected by the amplifier with full gain. As a result, the oscillation grows with time. See the earlier time part of the waveforms simulated with Agilent's Advanced Design Systems in Fig. 3.

As oscillation grows, V_A exhibits an increasingly larger swing, and so does V_B . When V_A rises, V_B follows up [Fig. 3], charging C_1 . The associated time constant is $\sim C_1/g_{m,1}$ where $g_{m,1}$ is the transconductance of N_1 . Since $1/g_{m,1}$ is arranged to be quite smaller than R_1 , R_1 hardly affects the

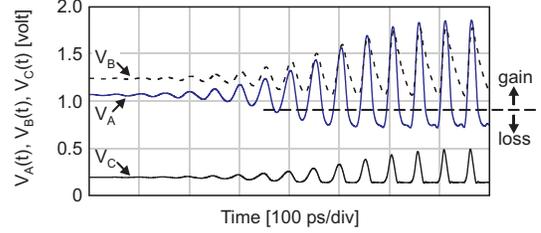


Fig. 3. Simulated waveforms.

time constant. When V_A falls, V_B follows down [Fig. 3], discharging C_1 . The discharging time constant is $\sim R_1C_1$, which is much larger than the charging time constant. $g_{m,1}$ does not affect the discharging time constant, as the discharged current cannot flow through N_1 . In sum, V_B rises quickly following V_A 's rise, as N_1 dumps charges on C_1 quickly, but V_B falls slowly when V_A falls, as discharging of C_1 through R_1 is slow. This behavior becomes conspicuous with growing oscillation [Fig. 3].

Therefore, as V_A falls significantly with growing oscillation, V_B cannot fall as fast, rendering V_A sufficiently below V_B to turn off N_1 . The critical level of V_A at which N_1 is turned off is shown as the horizontal broken line in Fig. 3. During the time within each oscillation period when V_A is below the critical level, the positive feedback is turned off due to the turn-off of N_1 , and the reflection amplifier produces a positive output resistance. Thus, the portion of the pulse arriving at the V_A node below the critical level is reflected with attenuation. On the other hand, for V_A above the critical level, N_1 is on and the positive feedback is activated, and the amplifier produces a negative output resistance. Therefore, the main portion of the pulse oncoming at the V_A node above the critical level is reflected with gain. In this way the level-dependent gain is gradually established. The level-dependent gain can also be evidenced by the plateau of V_C in Fig. 3 during V_A is below the critical level.

With growing oscillation, the lower part of V_A goes increasingly below the critical level [Fig. 3], enlarging the attenuation portion in the level-dependent gain, thus, decreasing the overall gain (which is subtraction of the attenuation below the critical level from the amplification beyond the level). Once the overall gain matches the line loss, steady state is reached. It is the level-dependent gain in steady state that enables formation and maintenance of the pulse shape. The level-dependent gain also stabilizes the steady-state oscillation by attenuating undesired perturbations (*e.g.*, noise) during the absence of the pulse, as they lie below the critical level [1]–[6]. The perturbations otherwise could grow into an additional pulse to corrupt the oscillation dynamics.

III. MEASUREMENTS

The die photo of the mode-locked oscillator integrated in GaAs technology using 70-nm metamorphic HEMTs

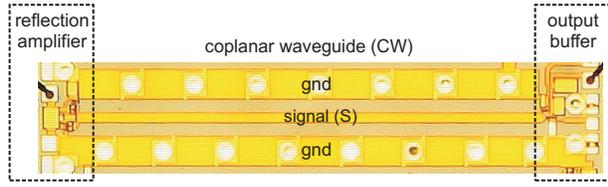


Fig. 4. Die micrograph. Area: 2.84 mm \times 0.49 mm.

(GaInAs/InAlAs) is shown in Fig. 4. The reflection amplifier dissipates 26 mW from a 2.0-V supply. The output buffer, which is for measurement with 50- Ω environment, consumes 18 mW from a 2.3-V supply.

We measured the oscillator signal in time domain using an Agilent 93-GHz 86100C sampling oscilloscope (50- Ω input port) in conjunction with 50- Ω RF probing (75-GHz 3-dB bandwidth). For the trigger input to the oscilloscope, a reference signal with a definite phase relation to the oscillator signal is needed to synchronize the oscilloscope to the oscillator signal. The maximum frequency the trigger input can admit is 15 GHz, which is lower than the pulse repetition rate, 18.7 GHz. Therefore, for the trigger input, we use a 9.35 GHz (half of 18.7 GHz) sinusoid produced by an Agilent 83650L generator, and supply the same 9.35 GHz sinusoid to the V_m port of the oscillator [Fig. 2] for subharmonic injection locking. The injection locking ensures a definite phase relation between the trigger and oscillator signal, and their frequency relation by an accurate factor of 2. V_m is tapped to the coplanar waveguide at the buffer end through a high impedance path consisting of a Schottky diode and a resistor [Fig. 2], which is to ensure full reflection at that line end. We confirmed no interference of the injection locking with the main signal dynamics (apart from fine phase control) by monitoring the oscillator output in an Agilent E4448A spectrum analyzer. In the phase noise measurement in frequency domain discussed later, we do neither need nor use injection locking, so that phase noise of the free-running oscillator can be measured.

Fig. 5(a) shows the measured oscillation signal at the output of the buffer. Waveform points from 64 consecutive acquisitions are averaged together by the oscilloscope to produce this focused waveform. The full width at half maximum (FWHM) of the pulse is 16 ps; the pulse repetition rate is 18.7 GHz. Its power spectrum calculated with respect to 50 Ω is shown in Fig. 5(b). The fundamental tone appears at 18.7 GHz. The spectral distribution over the multiple harmonics and their phase relation determine the pulse shape and width. Mathematical reconstruction of the measured time-domain signal demonstrates that the first 3 harmonic modes are locked with zero phase difference, while the 4th mode is ca. 120° out of phase from them. The 4th mode's behavior is because of the slight difference between the rise and fall time of the reflection amplifier. Our measurement band-limited by the RF probing (75 GHz 3-dB bandwidth) is not capable of

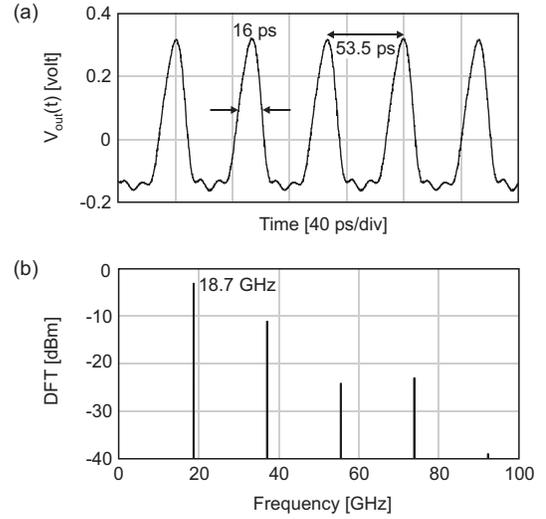


Fig. 5. (a) Measured steady-state oscillation at the buffer output. (b) Its power spectrum calculated with respect to 50- Ω .

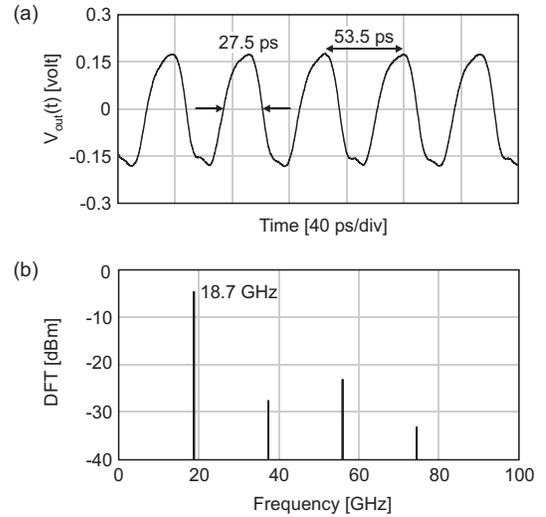


Fig. 6. (a) Measured near-sinusoidal oscillation. (b) Its power spectrum calculated with respect to 50- Ω .

measuring the 5th harmonic, which, however, would not be significant in pulse formation.

To further highlight the characteristic of the mode-locked signal via comparison, we produce a sinusoidal oscillation by altering the bias condition of the same oscillator. By increasing the supply of the amplifier from 2.0 to 2.4 V and injecting a dc current of 1 mA into the V_m node [Fig. 2], we convert the amplifier from the level-dependent gain mode to the full gain mode. The oscillator is not mode-locked any more, but generates a near-sinusoidal signal [Fig. 6(a)], which corresponds to a half-wavelength standing wave oscillation [12]. The corresponding power spectrum calculated with

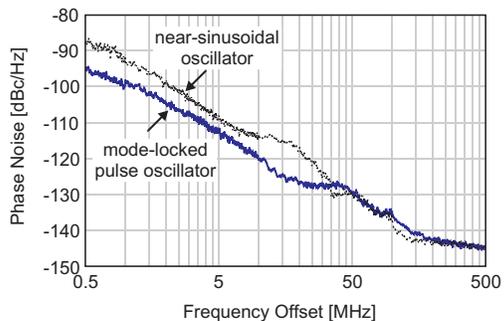


Fig. 7. Measured phase noise.

respect to 50Ω is shown in Fig. 6(b). The second harmonic mode of the sinusoidal standing wave oscillator [Fig. 6(b)] is 16.5 dB less in power than that of the mode-locked oscillator [Fig. 5(b)].

Figure 7 shows the phase noise of the mode-locked and sinusoidal standing wave oscillators (both free running), measured using the built-in phase noise measurement capability of an Agilent E4448A spectrum analyzer. The injection locking used to measure the time-domain signal is neither needed nor used in this frequency-domain phase noise measurement (actually injection locking should not be used to obtain the phase noise of the free running oscillators). In general, given the same amount of noise and total RF power of oscillation, the mode-locked oscillator's phase noise is lower than the sinusoidal oscillator's [7]. This tendency is well observed in Fig. 7 where the two oscillators have similar total RF output power and noise level. The mode-locked oscillator, our main design goal, has a phase noise of -99.5 dBc/Hz at 1-MHz offset. Measurements summarized in Table I emphasize the distinguishing characteristic of the mode-locked oscillator.

TABLE I
SUMMARY OF MEASUREMENTS.

	Mode-locked oscillator	Sinusoidal standing wave oscillator
f_0	18.7 GHz	18.7 GHz
Pulse width	16 ps	27.5 ps
Duty cycle	30%	51%
RF power (f_0)	-3.0 dBm	-4.5 dBm
RF power ($2f_0$)	-11.0 dBm	-27.5 dBm
P_{diss} (amp)	26 mW	38 mW
PN @ 1 MHz	-99.5 dBc/Hz	-93.1 dBc/Hz
PN @ 10 MHz	-121 dBc/Hz	-114 dBc/Hz

IV. CONCLUSION

Most works on electrical mode-locked oscillators have so far been mainly focused on concept proof with discrete design rather than speed enhancement with integrated design. This paper demonstrated the fastest electrical mode-locking

(18.7-GHz pulse repetition rate; 16-ps pulse width) by integrating a circuit that combines a coplanar waveguide and a reflection amplifier with level-dependent gain responsible for pulse formation/stability, and loss compensation. It also represents the first integration of the reflective-type electrical mode-locking. Further developments along this line may enable useful applications, e.g., high-speed sampling, time-domain metrology, and injection-lock based frequency synthesis, due to the nature of the electrical mode-locking, such as short pulse duration and inherent short-term frequency stability.

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