## 3.7 Dual-DLL-Based CMOS All-Digital Temperature Sensor for Microprocessor Thermal Monitoring

Kyoungho Woo[1], Scott Meninger[2], Thucydides Xanthopoulos[2], Ethan Crain[2], Dongwan Ha[1], Donhee Ham[1]

[1]Harvard University, Cambridge, MA, [2]Cavium Networks, Marlborough, MA

Today's microprocessors increasingly need on-chip temperature sensors for thermal and power management [1]. Since these sensors do not take part in the main computing activity but rather play the auxiliary, albeit important, role of temperature monitoring, their presence in terms of area, power, and design effort should be minimal, thus, all-digital sensors are desired. Temperature sensing based on temperature-dependent delays of inverters [2] could be suited for microprocessor applications, as it lends itself to digital implementation: by using a time-to-digital converter (TDC), an inverter delay can be compared to an absolute delay reference and converted to a digital temperature output [2] (Fig. 3.7.1). We report on an all-digital CMOS temperature sensor for microprocessor application, which also exploits temperature-dependent inverter delays within the TDC-based framework of Fig. 3.7.1. It, however, has two improvements over prior art of [2]. First, it removes the effect of process variation on inverter delays via calibration at one temperature point (instead of 2-point calibration of [2]), thus, reducing high volume production cost. Second, we use two fine-precision DLLs, one to synthesize a set of temperature-independent delay references in a closed loop, the other as a TDC to compare temperature-dependent inverter delays to the references. The use of DLLs simplifies sensor operation and yields a high measurement bandwidth (5kS/s) at 7b resolution, which could enable fast temperature tracking. This is in contrast to [2], where a counter-based cyclic TDC with an open-loop single delay-reference has a longer measurement time for a similar resolution.

Inverter delays vary with both temperature and process. Our sensor calibrates out the process dependency with a delay measurement at one temperature. This 1-point calibration is enabled by our observation that the inverter delay can be separated into a temperature-only-dependent part and a process-only-dependent part. The delay, $D$, of a CMOS inverter with equal PMOS and NMOS strengths may be expressed as

$$D = \frac{L}{W}\cdot\frac{C_L}{C_{OX}}\cdot\frac{1}{\mu}\cdot\frac{\ln(3-4V_{th}/V_{DD})}{V_{DD}(1-V_{th}/V_{DD})} \quad (1)$$

Temperature-dependent parameters are the mobility, μ, and threshold voltage, $V_{th}$, but $V_{th}$ weakly varies with temperature, so to the first order, only $\mu \propto T^{\alpha}$ ($\alpha$: constant) accounts for temperature dependence of $D$. To highlight this, eq. (1) can be rewritten as

$$D(T, P) = T^{\alpha}G(P)\ , \quad (2)$$

where $G(P)$ is what is left in $D$ after factoring out $T^{\alpha}$, and $P$ collectively denotes various process variations. $G(P)$ varies only with process variation. $T^{\alpha}$ varies only with temperature ($\alpha$ varies slowly with doping level, so it can be regarded as a constant in a given technology).

This separation of variables enables 1-point calibration. First we perform calibration once by measuring inverter delay $D(T_C,P) = T_c^{\alpha}G(P)$ at a known temperature $T_C$. Then we measure delay $D(T,P) = T^{\alpha}G(P)$ at an unknown temperature $T$ we seek to know. Division of $D(T, P)$ by $D(T_C, P)$ yields a *normalized delay* at $T$: $D_{norm}(T) \equiv D(T,P) / D(T_C,P) = (T/T_C)^{\alpha}$. Process dependency $G(P)$ disappeared due to the separation of variables. $D_{norm}(T)$ is a function of $T$ only, so it is reproducible across all process corners, serving as a good temperature representation. This is the foundation of our sensor operation with 1-point calibration.

Simulations validate this approach. Using 0.13μm CMOS technology, we simulated delays of two minimum-size inverters in series, with FO-2 load. Figure 3.7.2 shows simulated $D(T, P)$ and $D_{norm}(T)$ where $T_C$ = 50°C. While $D(T, P)$ varies across process corners, $D_{norm}(T)$ remains almost the same across corners. A dc-supply shift during measurement, which was not included in the above analysis, can cause significant temperature errors. Techniques to reduce this error are open to further study. In contrast, ac-supply variations are averaged out and cause insignificant error, as seen later.

We execute 1-point calibration and delay normalization using the circuit of Fig. 3.7.3. It contains an open-loop delay line, and a DLL that synthesizes temperature-independent-delay references. This *reference-DLL* (R-DLL) is locked to a crystal oscillator $x(t)$: each delay cell in the R-DLL has constant delay $\Delta_0$. MUX-1 taps a node in the R-DLL delay line: if the $N$-th cell's output is tapped, the delay from input $x(t)$ to output $d(t)$ of the R-DLL is $D_{DLL} = N\Delta_0$. This is our delay reference independent of temperature and process. $N$ can be altered to produce different reference delays. In the open-loop line, if the $M$-th cell's output is tapped by MUX-2, the delay between input $x(t)$ and output $c(t)$ is $D_{OL}(T,P) = T^{\alpha}G(P)M$ (eq. (2)), which varies with temperature and process.

In calibration mode at temperature $T_C$, we set $N = N_C$ to fix the reference delay at $D_{DLL} = N_C\Delta_0$. We then increase $M$ (MUX-2 setting) until $D_{OL}$ equals $D_{DLL}$ at $M = M_C$. This comparison of $D_{OL}$ to $D_{DLL}$ to find their *lock* at $M = M_C$ is done via the bang-bang phase detector in the middle of Fig. 3.7.3. So the entire architecture of Fig. 3.7.3 may be viewed as another DLL, which we call the *measuring DLL* (M-DLL; Fig. 3.7.4, top). At $M = M_C$, we have:

$$T_c^{-\alpha}G(P)M_C = N_C\Delta_0 \quad (3)$$

As $N_C\Delta_0$ and $T_c^{-\alpha}$ are constant, $G(P)M_C$ is constant across process corners ($M_C$ was so chosen), which is used later for delay normalization. This is the end of calibration, done in production line. MUX-2 has a hardwired setting, $M_C$, from now on.

Once 1-point calibration is complete, the sensor enters measurement mode. Temperature $T$ is unknown, thus, $D_{OL}$ of the hardwired open-loop line is an unknown delay, which the M-DLL measures by varying the reference delay $D_{DLL}$ of the R-DLL (bottom of Fig. 3,6,4). MUX-1 setting $N$ is varied until $D_{DLL}$ equals $D_{OL}$ at $N = N_m$. At this point, we have:

$$T^{-\alpha}G(P)M_C = N_m\Delta_0 \quad (4)$$

As $G(P)M_C$ was fixed in calibration mode (eq. (3)), we eliminate it in eq. (4) to obtain:

$$N_m = (T/T_C)^{-\alpha}N_C \quad (5)$$

$N_m$ is a function of $T$ only. Process dependency has been removed by the 1-point calibration that fixed $G(P)M_C$. $N_m$ is a digital output that faithfully represents $T$. $N_m$ corresponds to the normalized delay seen earlier.

Figure 3.7.5 shows the implemented architecture. It is essentially the same as Fig. 3.7.3, but has phase interpolators [3] to produce a 7 more phases between the input and output phase of a delay cell chosen by MUX-1 or MUX-2. The interpolators provide a fine-delay step of 20ps to map delay variations to 7b outputs to give sub-°C resolution. To attain $D_{DLL} = D_{OL}$ (calibration or measurement), we first alter MUX setting ($N$ or $M$) for coarse tuning, then, interpolator index $k$ (0 to 7) for fine tuning.

Figure 3.7.7. shows our sensor (0.12mm$^2$) fabricated in 0.13μm 1.2V digital CMOS. The clock $x(t)$ is 30MHz. Five chips, which represent process variation, were tested. In the first experiment, 1-point calibration ($T_C$ = 50°C) was done only in one chip, yielding $M_C$ for the chip. $M$ in each chip was fixed at this $M_C$, that is, the rest of the chips were not calibrated according to their own process variation. The top left of Fig. 3.7.6 shows R-DLL's delay index $N_m$ measured at from 0 to 100°C in steps of 10°C. Due to lack of proper calibration, $N_m$ vs. $T$ is not consistent among chips. In the second experiment, each chip received 1-point calibration appropriate to its process variation. Measured $N_m$ vs. $T$ is consistent among chips (Fig. 3.7.6, top right), validating our approach.

We obtain a master curve from Fig. 3.7.6 top right via 3rd-order fitting. The resolution estimated from the master curve is 0.66°C/LSB for 7b outputs. Chip-to-chip variations of $N_m$ (Fig. 3.7.6 top right) are converted to errors (Fig. 3.7.6 bottom), which fall within -1.8 to 2.3°C. The errors are largely due to the approximate nature of the separation of variables of eq. (2).

Each measured $N_m$ above is a number averaged over 100 data to remove jitters and supply fluctuations. The 100 data were sampled at 500kS/s for an effective conversion rate of 5kHz, taking 0.2ms to obtain an averaged $N_m$, with 1.2mW power dissipation (0.24μJ per averaged sample). The 1-point calibration, performed once at production test, takes about 0.5ms.

*References:*

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[2] P. Chen, C-C. Chen, C-C. Tsai, W-F. Lu, "A Time-to-Digital-Converter-Based CMOS Smart Temperature Sensor," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1642-1648, Aug. 2005.

[3] S. Sidiropoulos and M. Horowitz, "A semidigital dual delay-locked loop," *IEEE J. Solid-State Circuits*, vol. 32, no. 11, pp. 1683-1692, Nov. 1997.

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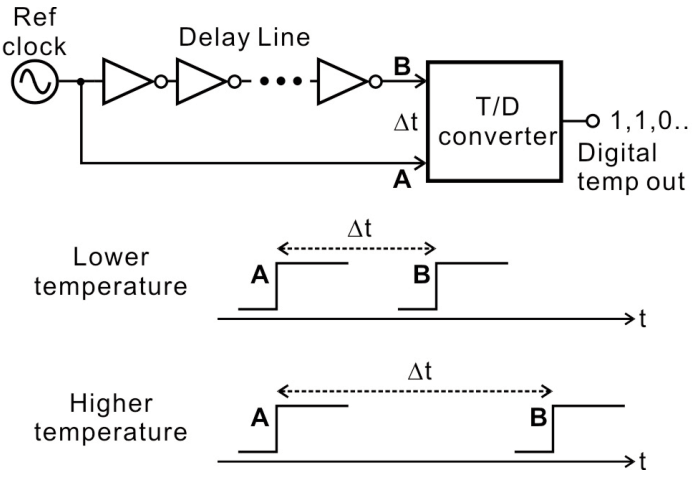


Figure 3.7.1: CMOS temperature sensor based on temperature-dependent delays of CMOS inverters.

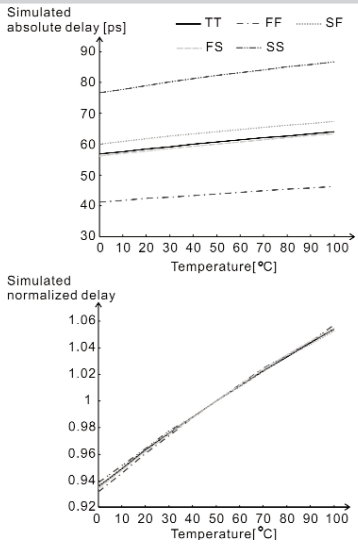


Figure 3.7.2: Simulated absolute (top) and normalized (bottom) inverter delays in different process corners.

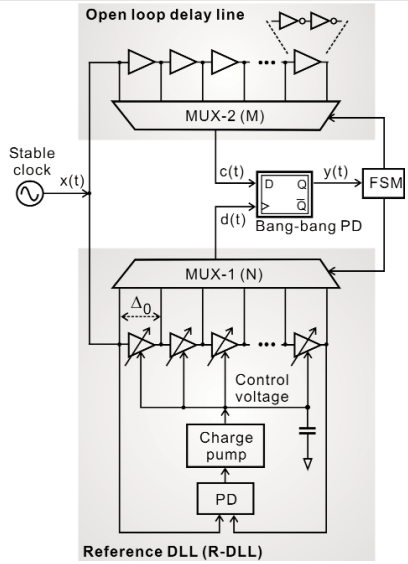


Figure 3.7.3: Basic architecture of DLL-based CMOS digital temperature sensor.

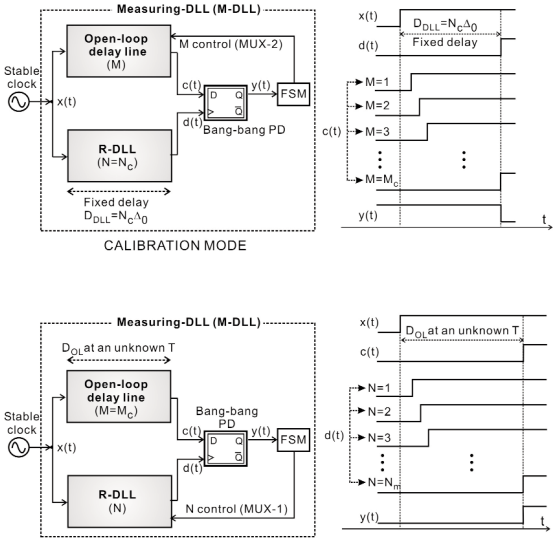


Figure 3.7.4: Calibration mode (top) and measurement mode (bottom).

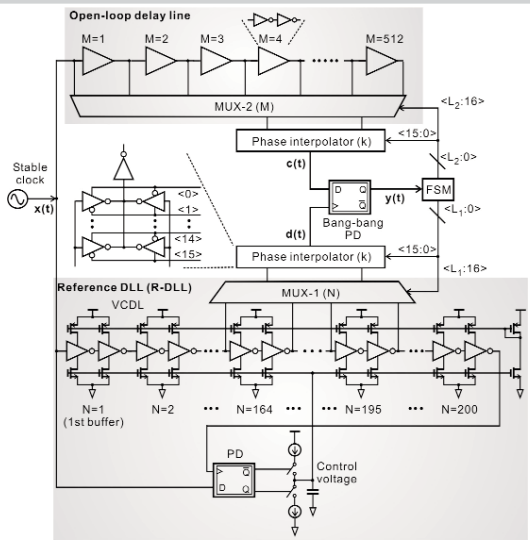


Figure 3.7.5: Detailed schematic of our DLL-based CMOS all-digital temperature sensor.

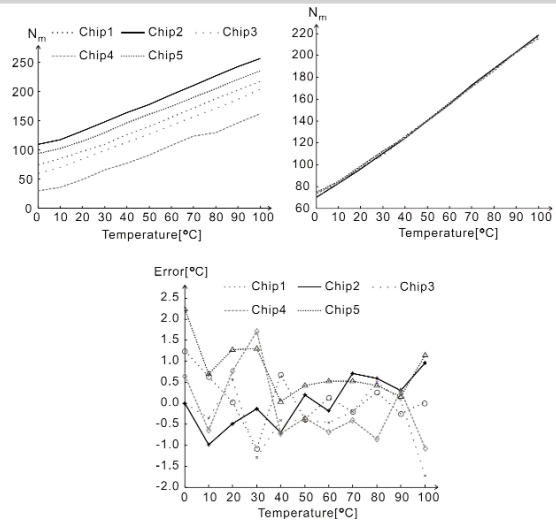


Figure 3.7.6: Measured $N_m$-vs-$T$ after no proper calibration (top left); measured $N_m$-vs.-$T$ after proper calibration (top right). $N_m$ takes into account the phase interpolator changing steps. Measurement errors (bottom).

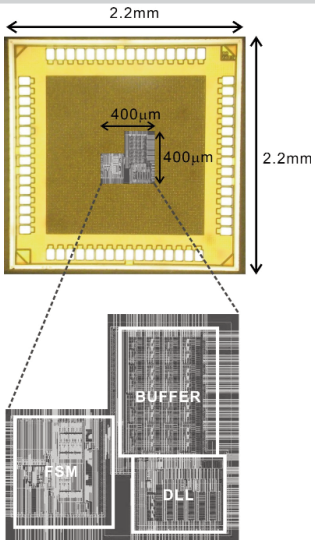


**Figure 3.7.7: Die micrograph. As metal fills block the circuit view, we overlay the circuit layout.**


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